MOSFET/IGBT DRIVERS THEORY AND APPLICATIONS

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By S.E. Nickols

Diablo Mountain Research LLC; 741 Buena Vista Place; Walnut Creek , CA 95497; Tel: 925-788-4807;

1. INTRODUCTION

Modern Power Electronics makes generous use of MOSFETs and IGBTs in most applications and, if the present trend is any indication, the future will see more and more applications making use of MOSFETs and IGBTs.

Although sufficient literature is available on characteristics of MOSFETs and IGBTs, practical aspects of driving them in specific circuit configurations at different power levels and at different frequencies require that design engineers pay attention to a number of aspects.

An attempt is made here to review this subject with some illustrative examples with a view to assist both experienced design engineers and those who are just initiated into this discipline .

1.1 MOSFET AND IGBT TECHNOLOGY

Due to the absence of minority carrier transport, MOSFETs can be switched at much higher frequencies. The limit on this is imposed by two factors: transit time of electrons across the drift region and the time required to charge and discharge the input Gate and 'Miller' capacitances.

IGBT derives its advantages from MOSFET and BJT. It operates as a MOSFET with an injecting region on its Drain side to provide for conductivity modulation of the Drain drift region so that on-state losses are reduced, especially when compared to an equally rated high voltage MOSFET.

As far as driving IGBT is concerned, it resembles a MOSFET and hence all turn-on and turn-off phenomena comments, diagrams and Driver circuits designed for driving MOSFET apply equally well to an IGBT. Therefore, what follows deals only with MOSFET models.

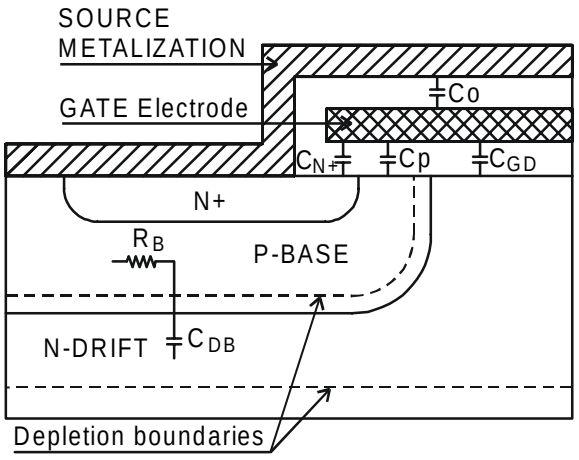


Fig. (1A) MOSFET cell internal structure

1.2 MOSFET MODELS AND CRITICAL PARAMETERS

Fig. (1A) shows the internal cell structure of a DMOS

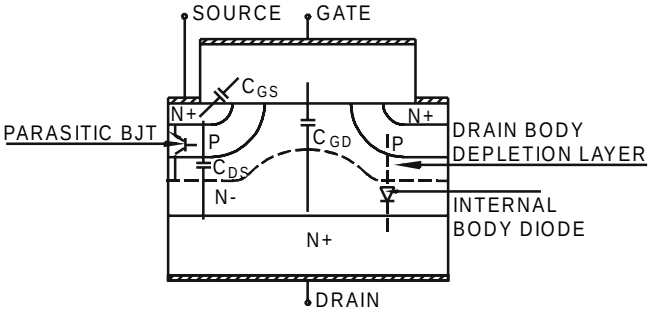


Fig. (1B) Cross sectional view of N-Channel MOSFET showing various inter-junction capacitances

MOSFET. As can be seen, the Gate to Source Capacitance consists of three components, namely, Cp, the component created by the Gate Electrode over the P-base region; $C_{N+,}$ due to the overlap of the Gate Electrode above the N+ source region and, C_O, arising due to the proximity of the Gate Electrode to the source metallization. In fact, all these are added to yield C_{GS}, which we call Gate-to-Source Capacitance. It is this total value of capacitance that needs to be first charged to a critical threshold voltage level $V_{GS(th)}$, before Drain Current can begin to flow. The Gate-to-Drain capacitance, C_{GD}, is the overlap capacitance between the Gate electrode and the N-drift Drain region. C_{GD} is sometimes referred to as the 'Miller' capacitance and contributes most to the switching speed limitation of the MOSFET. The junction capacitance between the drain to the P-Base region is C_{DS}. The P-Base region of the MOSFET is shorted to the N+ source. Fig. (2) shows curve of I_D (Drain Current) versus V_{GS} (Gate Source

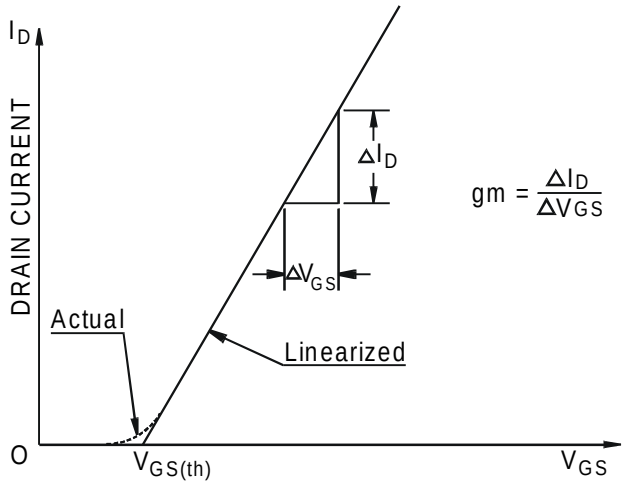


Fig. (2) Transfer characteristics of a power MOSFET

Voltage). The graph has a slope ($\triangle I_D / \triangle V_{GS}$) equal to g_m, which is called transconductance. Please note that the actual relationship between V_{GS} and I_D is shown by dotted line and it can be observed that in the vicinity of $V_{GS(th)}$, the relationship between V_{GS} and I_D is parabolic in nature:

$$I_D = K [V_{GS} - V_{GS(th)}]^2 \qquad \text{Eq.1.1}$$

However, for Power MOSFETs, it is appropriate to consider the relationship to be linear for values of V_{GS} above $V_{GS(th)}$. The manufacturer's data sheet value of $V_{GS(th)}$ is specified at 25 ^{o}C.

Fig. (3A) shows a symbol of N-Channel MOSFET and an equivalent model of the same with three inter-junction parasitic capacitances, namely: C_{GS}, C_{GD} and C_{DS}. I have shown all these as variable as they indeed are. For example the C_{GD}, decreases rapidly as the Drain to Source voltage rises, as shown in Fig. (3B). In Fig. (3B), the high value of C_{GD} is called C_{GDh}, while the low value of C_{GD} is termed C_{GDl}. Fig. (1B) shows another cross-sectional view of a MOSFET with all these capacitances. In addition, It also shows the internal body diode and the parasitic BJT.

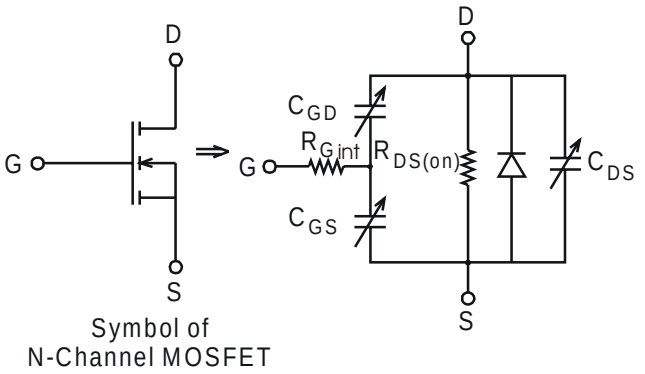


Fig. (3A) Symbol and equivalent circuit of a MOSFET

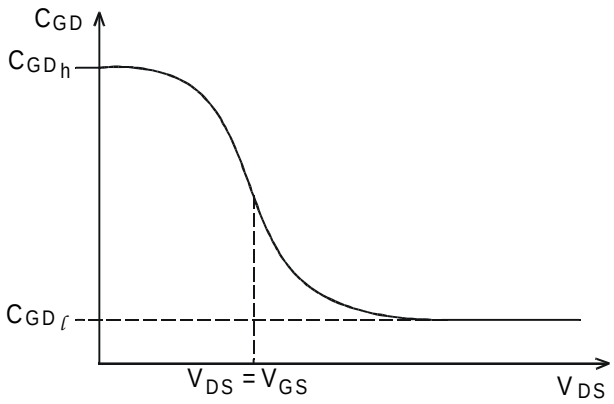


Fig. (3B) C_{GD} variation with respect to V_{DS}

1.3 Turn-on and Turn-off Phenomena

1.3.1 Turn-on Phenomenon

To understand Turn-on and Turn-off phenomena of the Power MOSFET, we will assume clamped inductive switching as it is the most widely used mode of operation. This is shown in Fig. (4A) and Fig. (4B). A model of MOSFET is shown with all relevant components, which play a role in turn-on and turn-off events. As stated above, MOSFET's Gate to Source Capacitance C_{GS} needs to be charged to a critical voltage level to initiate conduction from Drain to Source. A few words of explanation will help understand Fig. (4A) and Fig. (4B). The clamped inductive load is being shown by a current source with a diode D connected antiparallel across the inductor. The MOSFET has its intrinsic internal Gate resistance, called R_{Gint}. As described above, the inter-junction parametric capacitances (C_{GS}, C_{GD} and C_{DS}) are shown and connected at their proper points. V_{DD} represents the DC Bus voltage to the Drain of the MOSFET through the clamped inductive load. The Driver is supplied by Vcc of value Vp and its ground is connected to the common ground of V_{DD} and is returned to the Source of the MOSFET. The output from the Driver is connected to the Gate of the MOSFET through a resistor R_{Gext}.

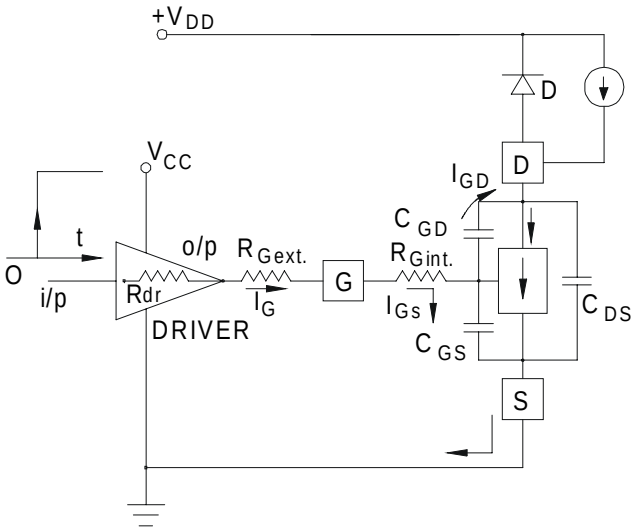


Fig (4A) A MOSFET being turned on by a driver in a clamped inductive load.

Now when a positive going pulse appears at the input terminal of the Driver, an amplified pulse appears at the output terminal of the Driver with an amplitude Vp. This is fed to the Gate of the MOSFET through R_{Gext}. As one can see the rate of rise of voltage, V_{GS}, over Gate and Source terminals of the MOSFET is governed by value of the total resistance in series ($R_{dr}+R_{Gext}+R_{Gint}$) and total effective value of capacitance ($C_{GS}+C_{GD}$). R_{dr} stands for the output source impedance of the Driver. R_{gext} is the resistance one generally puts in series with the Gate of a MOSFET to control the turn-on and turn-off speed of the MOSFET.

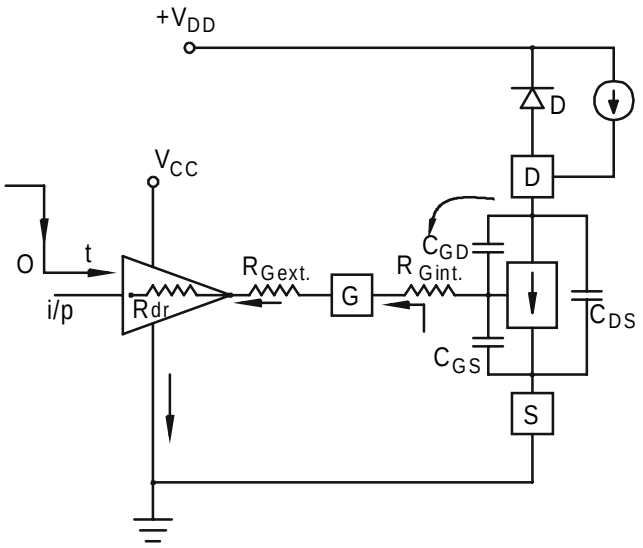


Fig. (4B) A MOSFET being turned off by a driver in a clamped inductive load.

The waveforms drawn in Fig. (5) show variation of different parameters with respect to time, so as to clearly explain the entire turn-on sequence. In Fig. (4A) and Fig. (4B), the Free Wheeling Diode D is assumed to be ideal with zero reverse recovery current. The waveforms shown in Fig. 5 are based on this assumption.

From time zero to t_1, (C_{GS}+C_{GDl}) is exponentially charged with a time constant T1=(R_{dr}+R_{Gext}+R_{Gint})x(C_{GS}+C_{GDl}), until Gate-to-source voltage reaches $V_{GS(th)}$. In this time period, neither the Drain voltage nor the Drain current are affected, i.e. Drain voltage remains at V_{DD} and Drain current has not commenced yet. This is also termed turn-on delay. Note that between 0 to t_1, as V_{GS} rises, I_{GS} falls exponentially, more or less like a mirror image of V_{GS}, because from the point of view of circuit analysis, it is an RC Circuit.

After time t_1, as the Gate-to-Source voltage rises above $V_{GS(th)}$, MOSFET enters linear region as shown in Fig. (2). At time t_1, Drain current commences, but the Drain to Source voltage V_{DS} is still at V_{DD}. However, after t_1, I_D builds up rapidly. As can be seen in Fig. (3B), from time t_1 to t_2, C_{GD} increases from C_{GDl} to C_{GDh} and current available from the Driver is diverted to charge this increased value of C_{GDh}. As we shall see later, this is the real test of a Driver- how fast it can charge C_{GDh} in addition to $C_{GS.}$

Between t_1 and t_2, the Drain current increases linearly with respect to V_{GS} . At time t_2, the Gate to Source voltage enters the Miller Plateau level. At time t_2, the Drain voltage begins to fall rapidly, while the MOSFET is carrying full load current. During the time interval, t_2 to t_4, V_{GS} remains clamped to the same value and so does I_{GS}. This is called the Miller Plateau Region. During this interval most of the drive current available from the driver is diverted to discharge the C_{GD} capacitance to enhance rapid fall of Drain to Source voltage. Only the external impedance in series with V_{DD} limits drain current.

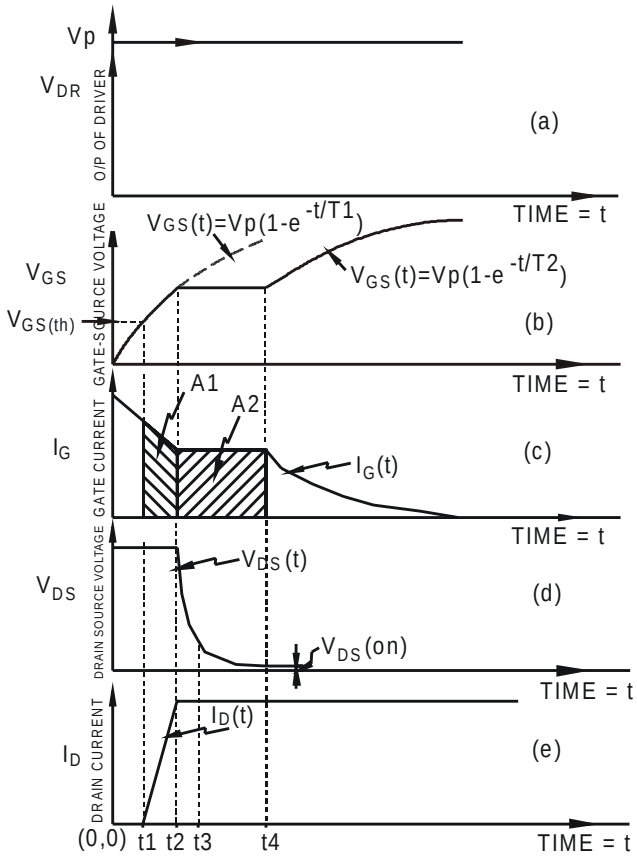


Fig. (5) MOSFET turn on sequence

Beyond t_4, V_{GS} begins to exponentially rise again with a time constant T_2 = (R_{dr}+R_{Gext}+R_{Gint})x(C_{GS}+C_{GDh}). During this time interval the MOSFET gets fully enhanced, the final value of the V_{GS} determining the effective $R_{DS(on)}$. When V_{GS} reaches its ultimate value, V_{DS} attains its lowest value, determined by V_{DS}= I_{DS}x $R_{DS(on)}$.

In Fig. (5), A1 represents area of I_G curve from time t_1 to t_2. This represents charge on (C_{GS} +C_{GD}), as it is the integration of Gate current over a time period. Similarly A2 represents charge on $C_{GD,}$ because it is an integration of I_G with respect to time from t_2 to t_3, during which time the Miller effect is predominant.

If one considers diode 'D' not to be ideal, then the reverse recovery of the diode will influence the turn on behavior and the waveforms would look like what is drawn in Fig. (6). As the diode undergoes reverse recovery, you can see a hump in the waveform of V_{GS} as well as $I_{D.}$ This occurs at and around time t_2.

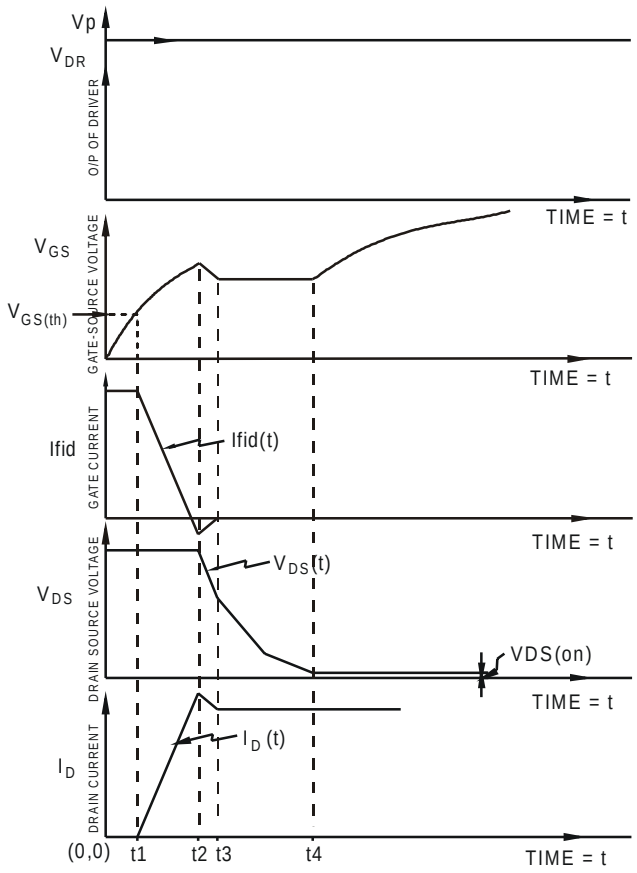


Fig. (6) MOSFET turn on sequence showing the effect of body diode reverse recovery.

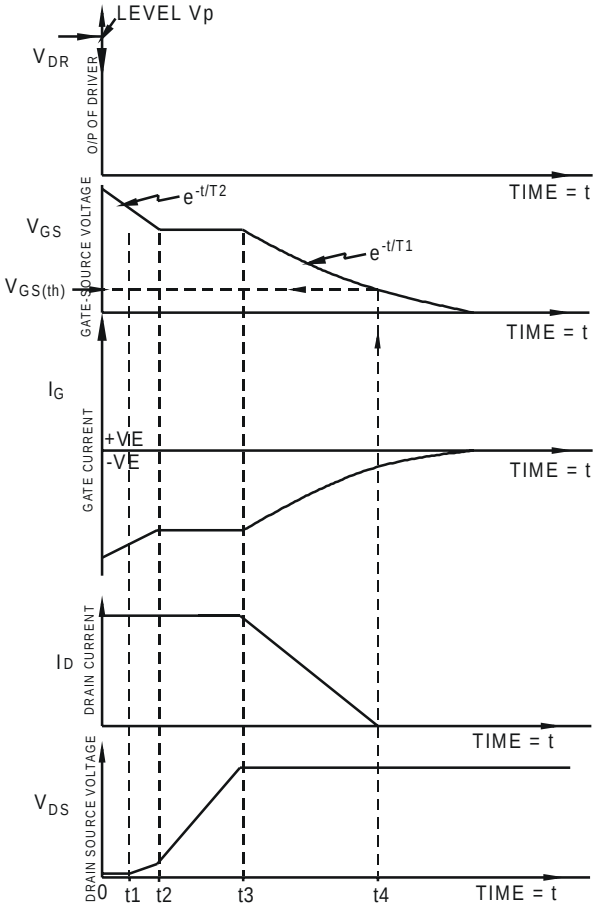


Fig. (7) MOSFET turn off sequence

1.3.2. The Turn-off Phenomenon:

The turn-off phenomenon is shown in Fig. (7). As can be expected, when the output from the Driver drops to zero for turning off MOSFET, V_{GS} initially decays exponentially at the rate determined by time constant T_2= $(R_{dr}+R_{Gext}+R_{Gint})x(C_{GS}+C_{GDh})$ from time 0 to t_1; however, after t_4, it decays exponentially at the rate determined by T1 = (Rdr+RGext+RGint)x(CGS+C_{GDI}). Please note that the first delay in the turn off process is required to discharge the C_{ISS} capacitance from its initial value to the Miller Plateau level. From t = 0 to t = t_1, the gate current is flowing through C_{GS} and C_{GD} capacitances of MOSFET. Notice that the drain current I_D remains unchanged during this time interval, but the Drain Source voltage V_{DS} just begins to rise. From t_1 to t_2 , V_{DS} rises from I_D x $R_{DS(on)}$ towards its final off state value of $V_{DS(off)}$, where it is clamped to the DC Bus voltage level by the diode in the clamped inductive switching circuit being studied. This time interval also corresponds to the Miller region as far as the gate voltage is concerned as mentioned above, which keeps V_{GS} constant.

During the next time interval, the V_{GS} begins to fall further below $V_{GS(th)}$. C_{GS} is getting discharged through any external impedance between Gate and Source terminals. The MOSFET is in its linear region and Drain current I_D drops rapidly towards zero value. Remember that the Drain Voltage V_{DS} was already at its off state value $V_{DS(off)}$ at the beginning of this interval. Thus at t_4, the MOSFET is fully turned off.

Manufacturer's Data Sheet of MOSFET gives values of C_{ISS}, C_{RSS} and C_{OSS}. The following relationships help relate these to inter-junction parasitic capacitances described so far:

$$C_{GD} = C_{RSS}$$
$$C_{GS} = C_{ISS} - C_{RSS} \qquad \text{Eq. 1.2}$$
$$C_{OS} = C_{OSS} - C_{RSS}$$

As C_{GD} and C_{DS} capacitances are dependent on V_{DS}, Data Sheet values are valid only at specified test conditions. To compute average effective values of these capacitances, one can use following formulae, which determines these based on required charge to establish voltage changes across these capacitances:

$$\text{Effective } C_{GD} = 2(C_{RSS\ specified})(V_{DS.specified}/V_{DS.off})^{1/2}$$
$$\text{Effective } C_{OSS} = 2(C_{OSS\ specified})(V_{DS.specified}/V_{DS.off})^{1/2} \qquad \text{Eq.1.3}$$

1.4 POWER LOSSES IN DRIVERS AND DRIVEN MOSFET/IGBT

For determining the power loss in a Driver while driving a power MOSFET, the best way is to refer to the Gate Charge Q_G vs. V_{GS} curve for different values of $V_{DS(off)}$.

$$P_{GATE} = V_{CC} * Qg * f_{sw} \qquad \text{Eq. 1.4}$$

wherein Vcc is the Driver's supply voltage, Qg is the total Gate Charge of the MOSFET being driven and f_{sw} is the switching frequency. It is prudent then to choose a MOSFET with lower value of Qg and it is here that IXYS' series of low Gate Charge MOSFETs with a suffix 'Q' are preferred because they as well as the drivers incur lower losses.

As far as switching losses in a MOSFET are concerned, as can be seen in Fig. (5), Fig. (6) and Fig. (7), there are some short time-intervals, during which finite V_{DS} and finite I_D coexist, albeit momentarily. When this happens during turn-on, the actual integration:

$$\int V_{DS}(t)\, I_D(t)\, dt \qquad \text{Eq. 1.5}$$

is defined as Turn-On switching energy loss. Likewise, during turn-off, when finite values of I_D and V_{DS} coexist, integration of:

$$\int V_{DS}(t) I_D(t) dt \qquad \text{Eq. 1.6}$$

is called Turn-off switching energy loss in a MOSFET. Amongst the responsible parameters determining these switching energy losses, C_{ISS}, C_{OSS} and C_{RSS} affect the turn-on and turn-off delays as well as turn-on and turn-off times.

For an IGBT, it would be similarly shown that:

$$\int V_{CE}(t) I_C(t) dt \qquad \text{Eq. 1.7}$$

represents switching energy loss. Needless to emphasize that the time interval for these integrals would be the appropriate time during which finite values of I_D and V_{DS} or V_{CE} and I_C coexist in a MOSFET or IGBT respectively. Average switching energy lost in the device can be computed thusly:

MOSFET: $Ps = 1/2 * V_{DS} * I_D * fsw * (ton+toff)$ Eq. 1.8

IGBT: $Ps = 1/2 * V_{CE} * I_C * fsw * (ton+toff)$ Eq. 1.9

Main emphasis in modern Power Electronics is on reducing total losses dissipated in devices and subsystems for higher operating efficiency and achieving more compact designs, reducing volume and weight of resultant systems. Thus, operation at higher and higher switching frequencies is now a necessity, and as a result, switching losses predominate in power-loss-budget in semiconductor switches. Reducing switching losses then becomes the single most crucial goal. Keeping this goal in mind, the entire line of IXYS MOSFET/IGBT Drivers are designed to facilitate the design of drive circuits that yield fast rise and fall times.

2. TYPES OF DRIVERS

2.1 IC DRIVERS

Although there are many ways to drive MOSFET/IGBTs using hard wired electronic circuits, IC Drivers offer convenience and features that attract designers. The foremost advantage is compactness. IC Drivers intrinsically offer lower propagation delay. As all important parameters are specified in an IC Driver, designers need not go through time consuming process of defining, designing and testing circuits to drive MOSFET/IGBTs.

2.2 TECHNIQUES AVAILABLE TO BOOST CURRENT OUTPUTS

Totem pole stage with N-Channel and P-Channel MOSFETs can be used to boost the output from an IC Driver. The disadvantage is that the signal is inverted and also there exists shoot through when common gate voltage is in transition.

Totem pole arrangement using matched NPN-PNP transistors, on the other hand, offer many advantages, while boosting the output currents from IC Drivers. Shoot through phenomenon is absent in this case. The pair of transistors protects each other's base-emitter junctions and handle current surges quite well. One such arrangement is shown in Fig. (14). Here Q1 is a NPN transistor, while Q2 is a matched PNP transistor with appropriate collector current rating and switching speed to satisfy Drive requirement for the High Power IGBT. Another feature added is –ve bias for guaranteed fast switch-off even in electrically noisy environment. This is done, by utilizing power supply with +15 and –5 Volts output, whose common ground is connected to the IGBT emitter.

IXDD408 is a very high speed IC Driver with extremely short rise and fall times and propagation delays. Its Vcc rating is 25 VDC and can actually deliver 8 Amperes peak output current. The arrangement shown in Fig. (14) does a few more things in addition to boosting the output current still higher. It allows one to choose different Turn-On and Turn-Off times by choosing different values of R_{gon} and $R_{goff.}$ It allows for incorporating –ve bias for reasons explained above. A pair of 18V Zener diodes with their cathodes connected together, protects the Gate-Emitter Junc-

tion of IGBT from voltage spikes.

2.3 TECHNIQUES TO GENERATE –Ve BIAS DURING TURN-OFF

Importance of –ve bias during turn-off for practically all semiconductor switches cannot be overemphasized, as one may recall from the days of Bipolar transistors. This helps to quickly remove any charge on the C_{GS} and C_{GD} in the case of MOSFETs and IGBTs, thus considerably accelerating turn-off.

It is important to understand that turn-on speed of a MOSFET or IGBT can be increased only up to a level matched by the reverse recovery of rectifiers or diodes in a power supply, because in an inductive clamped load (most common), turn-on of a MOSFET or IGBT coincides with turn-off (or reverse recovery completion) of the rectifier diode. Any turn-on faster than this does not help. Too fast a turn-on could also cause oscillation in the Drain or Collector current. However, it is always beneficial to have a Driver with intrinsic low turn-on time and then be able to tailor this with a series gate resistor.

Turn-off phenomenon, on the other hand, does not have to wait for any other component in the subsystem. It is here that any enhancement technique can be utilized. Although IXYS drivers themselves feature extremely low turn-on and turn-off times, arrangement to provide –ve bias during turn-off helps still faster turn-off and prevents false turn on even in electrically noisy environment.

Fig. (12C) demonstrates one way of generating –ve bias during turn-off. Fig. (18) shows how to generate –ve bias in a transformer coupled Drive circuit arrangement. Here Zener diode can be chosen of appropriate voltage for giving that much –ve bias (plus one diode drop) during turn-off. Another unique feature of circuit in Fig.(18) is its ability to maintain exact pulse wave shape across Gate and source. In Fig. (16) a method of using isolated DC to DC converter with outputs of +15 and –5 V is used to power IXDD414, while by connecting isolated ground of this DC to DC Converter to the emitter of the IGBT being driven, –5 V of –ve bias during turn-off is ensured.

2.4 NEED FOR UNDER-VOLTAGE PROTECTION

Fig. (2) shows a transfer characteristics (I_D vs. V_{GS}) of a MOSFET. As can be seen for values of V_{GS} below $V_{GS(th)}$ the drain current is negligible, but in this vicinity, the device is in its linear (Ohmic) region and concurrent application of large values of V_{DS} could cause considerable amount of localized heating of the junction. In short, when a MOSFET is being used as a switch, any operation in its linear region could cause overheating or device failure. Bringing the MOSFET quickly into its saturation from its off-state is the Driver's job. And, if Vcc is below the minimum required value, linear operation can ensue to the detriment of MOSFET. I hasten to add, however, that most PWM ICs, controller ICs and microcomputer ICs have this protection feature built-in and, if sharing the same Vcc bus, the Driver IC gets the benefit of this function being implemented elsewhere in the subsystem.

2.5 OVERLOAD/SHORT CIRCUIT PROTECTION

Any operation of MOSFET/IGBT outside the Safe Operating Area (SOA) could cause overheating and eventual device failure and should be prevented by an electronic active monitoring and corrective arrangement.

Load or current sensing could be done by either a Hall Effect Sensor or by a Shunt resistor in series with source/emitter terminal. The voltage picked up, which is proportional to current, is low pass filtered and then compared to a preset limit. The comparator output could initiate turn-off of MOSFET/IGBT. A circuit to detect overload/short circuit is shown in Fig. (16), where the output FAULT will go low when it occurs.

All IXDD series of Drivers have an ENABLE pin, which, when driven low, say, by the FAULT output from this comparator, puts the final N-Channel and P-channel MOSFETs of the IXDD Driver in its TRISTATE mode. This not only stops any output from the Driver, but also provides an environment for implementing soft turn-off. There are two ways of doing this. Just by connecting a resistor of appropriate value from Gate to source/emitter, the C_{GS} gets discharged through this resistor and, depending on the value of the connected resistor, soft turn-off of any duration can be achieved. Another way, as shown in the Fig. (9), is to use a signal MOSFET Q1 to pull down the Gate, when short circuit is detected. The resistor in series with this signal MOSFET determines the time duration of this soft turn-off. Soft turn-off helps protect IGBT/MOSFET from any voltage transients generated due to LdI_C/dt (or LdI_D/dt) that could otherwise bring about avalanche breakdown. The PC board layout for this circuit is shown in Fig. (10).

For an IGBT, Desat detection (Desat = Desaturation of forward voltage drop) is a method used for short circuit/overload protection. When short circuit/overload occurs, the forward voltage drop of the IGBT (V_{CE}) rises to disproportionately high values. One must ignore the initial turn-on rise in V_{CE}, when output from Driver has still not risen to high enough value. Nevertheless, when V_{CE} rises to a level of, say, 7 Volts, in presence of sufficient Gate Drive voltage, it means the collector current I_C has risen to a

disproportionately high value, signaling overload. When a voltage level higher than 6.5 Volts is detected, Gate signal can be softly turned off, resulting into soft turn-off of the IGBT. Fig. (16) shows how Desat feature can be wired into a total Driver Circuit, using also other features, such as Opto-isolation and –ve turn-off bias.

3. HIGH SIDE DRIVING TECHNIQUES

3.1 EMPLOYING CHARGE-PUMP AND BOOTSTRAP METHODS

For driving the upper MOSFET/IGBT in a phase leg employed in a bridge topology, a buck converter or a 2-transitor forward converter, low side drivers cannot be used directly. This is because the source/emitter of upper MOSFET/IGBT is not sitting at ground potential.

Fig. (12A) shows how a charge pump creates a higher Vcc to be used for the driver IC for the Upper MOSFET/IGBT. Here the pair of N-Channel and P-Channel MOSFETs acts as switches, alternately connecting incoming supply voltage to output through capacitors and Schottky diodes, isolating it and almost doubling it. Switching frequency in several hundred Kilohertz is used and, therefore, low ripple isolated output voltage is available as DC Supply for the Driver of Upper MOSFET/IGBT. Fig. (12C) illustrates how one IXDD404 can be used as charge pump, delivering 350 mA, and one IXDD408 as a Driver giving +/- 8 Amps, in conjunction with IXBD4410 and IXBD4411, for driving a phase leg of two IXFX50N50 MOSFETs. Fig. (12D) shows how a charge pump delivering as much as 500 mA can be constructed using one IXDD404; and by utilizing one IXDD414, one can boost the output from IXBD4410 and IXBD4411 to +/- 14Amps for driving Size 9 high power MOSFETs and IGBTs or even MOSFET/IGBT modules in phase leg configuration.

Another method is the Bootstrap Technique as shown in Fig. (12B). The basic bootstrap building elements are the level shift circuit, bootstrap diode DB, level shift transistor Q1, bootstrap capacitor CB and IXDD408 or IXDD414. The bootstrap capacitor, IXDD408/IXDD414 driver and the gate resistor are the floating, source-referenced parts of the bootstrap arrangement. The disadvantages of this technique are longer turn-on and turn-off delays and 100% duty cycle is not possible. Additionally the driver has to overcome the load impedance and negative voltage present at the source of the device during turn-off.

3.2 ACHIEVING GALVANIC ISOLATION BY USING OPTO-COUPLERS TO DRIVE UPPER MOSFET/IGBT

For driving high side MOSFET/IGBT in any topology, opto-couplers can be used with following advantages:

1. They can be used to give a very high isolation voltage; 2500 to 5000 Volts of isolation is achievable by use of properly certified opto-couplers.

2. Signals from DC to several MHz can be handled by opto-couplers.

3. They can be easily interfaced to Microcomputers or other controller ICs or any PWM IC.

One disadvantage is that the opto-coupler adds its own propagation delay. Another disadvantage of using an opto-coupler is that separate isolated power supply is required to feed the output side of the opto-coupler and the driver connected to it. However, isolated DC to DC Converters with few thousand Volts of isolation are readily available. These can be used to supply isolated and regulated +ve 15 V and –ve 5V to the output side of the opto-coupler and the Driver IC for driving Upper MOSFET/IGBT as is shown in Fig. (16) and Fig. (17). As can be seen, identical chain of opto-coupler, Driver and DC to DC Converters are used for even lower IGBTs. This is to guarantee identical propagation delays for all signals so that their time of arrival at the Gate of IGBT bear the same phase relationships with one another as when they originated in the microcomputer.

3.3 USE OF TRANSFORMERS TO OBTAIN GALVANIC ISOLATION IN DRIVING UPPER MOSFET/IGBT

Using transformers to achieve galvanic isolation is a very old technique. Depending on the range of frequencies being handled and power rating (voltage and current ratings and ratios), transformers can be designed to be quite efficient. The gate drive transformer carries very small average power but delivers high peak currents at turn-on and turn-off of MOSFET/IGBT.

While designing or choosing a Gate Drive transformer, the following points should be kept in mind:

1. Average power being handled by the transformer should be used as a design guideline. Margin of safety should be taken into account, keeping in mind maximum volt-second product and allowing for worst case transients with maximum duty ratio and maximum input voltage possible.
2. Employing bifilar winding techniques to eliminate any net DC current in any winding. This is to avoid core saturation.
3. If operation in any one quadrant of B-H loop is chosen, care should be taken for resetting the core.

Advantages of employing transformers for Gate Drive are:

1. There is no need for any isolated DC to DC Converter

for driving an upper MOSFET/IGBT .
2. There is practically no propagation delay time in a transformer to carry signals from primary side to the secondary side.
3. Several thousand volts of isolation can be built-in between windings by proper design and layouts.

The disadvantages of using transformers for Gate Drive are:

1. They can be used only for AC signals.
2. Large duty ratios cannot be handled by the transformer without being saturated by net DC, unless AC coupling capacitors are employed in series.

Two examples of gate Drive circuits, using transformers follow. In Fig. (15), a phase shift controller outputs its signals to the IXDD404 Dual Drivers, which in-turn, feed the transformers. The secondary windings of these transformers are coupled to the Gates of upper and lower MOSFETs in a "H" Bridge topology. Fig. (18) shows another transformer coupled Gate Drive circuit employing DC restore technique to maintain same waveshape of original signal with added feature of -ve bias offered using a Zener in series with a fast diode across secondary.

4.0 IXYS LINE OF MOSFET/IGBT DRIVERS

IXYS Corporation offers the following MOSFET/IGBT Drivers:

1. IXBD4410 and IXBD4411 Half Bridge Driver Chipset
2. IXDD404 Dual 4 Amp Ultrafast Driver
3. IXDD408 Single 8 Amp Ultrafast Driver
4. IXDD414 Single 14 Amp Ultrafast Driver
5. IXDD415 Dual 15 Amp Ultrafast Driver

4.1 IXBD4410 and IXBD4411 Half Bridge MOSFET/ IGBT Driver Chipset

This chipset is best suited to applications in Half Bridge, Full Bridge and 3 Phase Bridge topologies. Here the IXBD4410 is wired as a full-featured Low-Side Driver, while IXBD4411 is wired as a full-featured High-Side Driver. Together, they make up a stand alone Driver System for Phase leg of any of the above mentioned Bridge Configurations. The suggested wiring diagram is shown in Fig. (11). Likewise, the wiring diagram is to be repeated for each phase leg and hence one needs two such cards for "H" Bridge and three such cards for 3-Phase Bridge.

As can be seen in this schematic, to obtain galvanic isolation, it uses one ferrite core transformer for sending drive signals to IXBD4411 and another ferrite core transformer for receiving fault and status signals from IXBD4411. T1 represents both these transformers housed in one IC type package. To avoid saturation, capacitors are placed in series with each primary winding to which AC (time-varying signals) are transmitted. 1200 Volts of isolation barrier is built in.

Both IXBD4410 and IXBD4411 are feature-rich Drivers. These include:

1. Undervoltage and overvoltage lockout protection for Vcc;
2. dV/dt immunity of greater than ± 50 V/ns;
3. Galvanic isolation of 1200 Volts (or greater) between low side and high side;
4. On-chip negative gate-drive supply to ensure MOSFET/IGBT turn-off even in electrically noisy environment;
5. 5 volt logic compatible HCMOS inputs with hysteresis;
6. 20ns rise and fall times with 1000 pF load and 100 ns rise and fall times with 10000 pF load;
7. 100 ns of propagation delay;
8. 2 Ampere peak output Drive Capability;
9. Automatic shutdown of output in response to overcurrent and/or short-circuit;
10. Protection against cross conduction between upper and lower MOSFET/IGBT;
11. Logic compatible fault indication from both low and high-side drivers.

Higher current MOSFET/IGBTs require higher drive currents, especially for operating them at high switching frequencies. For these applications, one can use IXDD408 or IXDD414, either in stand-alone mode or in conjunction with IXBD4410 and IXBD4411. It is easy to realize now that one can easily get all the facilities of feature-rich IXBD4410 and IXBD4411 and when higher drive current capability is called for, use them in conjunction with IXDD408 or IXDD414. In case of a low-side MOSFET/ IGBT, it is simple to use IXDD408 or IXDD414 alone. One such example is given in Fig. (11).

For driving upper MOSFET/IGBT of a phase leg, one of the approaches is to employ a charge pump. Two such application circuit schematics are shown in Fig. (12C) and Fig. (12D). In Fig. (12C) output from IXBD4410/4411 is boosted up to ± 8 Amps using IXDD408 and the charge pump output is boosted to 350 mA, using one driver of IXDD404 for driving IXFK48N50 (rated at Id=48 Amps and Vd = 500 Volts). In Fig. (12D), the output from IXBD4410/ 4411 is boosted up to ±14 Amps by IXDD414 to drive a Size 9 MOSFET IXFN80N50 (rated at Id = 80 Amps and Vd = 500 Volts). IXDD404 can still adequately provide 500 mA for the charge pump circuit.

4.2 GENERAL REMARKS ABOUT IXDD SERIES OF DRIVERS

The most important strength of these Drivers is their ability to provide high currents needed to adequately drive today's and tomorrow's large size MOSFETs and IGBTs. This is made possible by devoting a large portion of the silicon die area to creating high current (NMOS and PMOS) output stage. Another important feature of these Drivers is that there is no cross conduction, thus giving almost 33% lower transition power dissipation.

In addition, all these Drivers incorporate a unique facility to disable output by using the ENABLE pin. With the exception of the IXDD408, the ENABLE pin is tied high internally. When this pin is driven LOW in response to detecting an abnormal load current, the Driver output enters its Tristate (High Impedance State) mode and a soft turn-off of MOSFET/IGBT can be achieved. This helps prevent damage that could occur to the MOSFET/IGBT due to LdI/dt overvoltage transient, if it were to be switched off abruptly, "L" representing total inductance in series with Drain or Collector. A suggested circuit to accomplish this soft turn off upon detecting overload or short circuit is shown in Fig. (9). It is also possible to do this by an independent short circuit/overload detect circuit, which could be a part of the PWM or other controller IC. All one needs to do is to take output signal (FAULT) from such a circuit and feed it into the ENABLE pin of Driver. A resistor R_P connected across Gate and Source or Gate and Emitter (as the case may be) would ensure soft turn-off of the MOSFET/IGBT, turn-off time being equal to $R_P(C_{GS}+C_{GD})$

Detailed specifications of these IXDD series of Drivers are available on web site www.ixys.com under heading: "ICs". All IXDD series of IXYS MOSFET/IGBT Drivers are Low-Side Drivers, but with techniques covered in this Application Note, one can use them as High-Side Drivers as well. Evaluation Printed Circuit Boards are also available.

4.2.1 IXDD404

IXDD404 is a dual 4 Ampere Driver, which comes in handy in many circuits employing two MOSFETs or IGBTs. It could also be used for two MOSFETs/IGBTs connected in phase leg, provided the voltage level is below 25 VDC. While using High Voltage DC Supplies for driving Phase leg, H-Bridge or 3 Phase Bridge Circuits, some technique for achieving galvanic isolation of upper MOSFET/IGBT Drivers is required, in addition to making provision for isolated power supplies.

Fig. (15) shows an interesting application for IXDD404 in a Phase Shift PWM Controller application, in which galvanic isolation is obtained by using ferrite core Gate Drive Transformers. Note that this Controller operates at a fixed frequency. Turn-off enhancement is achieved by using local PNP transistors.

For a vast number of low and medium current MOSFETs and IGBTs, IXDD404 provides a simple answer for driving them.

4.2.2 IXDD408 AND IXDD414

IXDD408 is eminently suitable for driving higher current MOSFETs and IGBTs and IXDD414 can drive larger size MOSFET/IGBT Modules. Many circuit schematics applying these in various topologies are possible and some of these are shown in different figures in this application note.

The 5 pin TO-263 surface mount version can be soldered directly on to a copper pad on the printed circuit board for better heat dissipation. It is possible then to use these high current drivers for very high frequency switching application, driving high current MOSFET modules for a high power converter/inverter.

Fig. (8) shows a basic low side driver configuration using IXDD408 or IXDD414. C1 is used as a bypass capacitor placed very close to pin No. 1 and 8 of the Driver IC. Fig. .(13) shows a method to separately control the turn on and turn off times of MOSFET/IGBT. Turn-on time can be adjusted by R_{gon}, while the turn-off time can be varied by R_{goff}. The diodes in series are fast diodes with low forward voltage drop. The 18V, 400mW Zener diodes protect the Gate-Emitter junction of the IGBT. A careful layout of the PCB, making shortest possible length between pin Nos.6 and 7 and IGBT Gate and providing generous copper surface for a ground plane, helps achieve fast turn-on and turn-off times without creating oscillation in the Drain/ Collector current.

Fig. (13) shows another arrangement and includes a method for faster turn-off using a PNP transistor placed very close to the MOSFET Gate and Source. It is a good practice to tie the ENABLE pin of drivers to Vcc through a 10K resistor. This ensures that the driver always remains in its ENABLED mode except when driven low due to a FAULT signal. Again this FAULT signal puts these two drivers into their TRISTATE output mode.

Fig. (14) shows a method to boost output from IXDD408 to a much higher level for driving very high power IGBT module. Here the turn-on and turn-off times can be varied by choosing different values of resistors, R_{gon} and R_{goff}. To provide –ve bias of 5 Volts, the IGBT emitter is grounded to the common of +15V and –5V power supply, which feeds +15V and –5 v to the IXDD408. Notice that the incoming signals must also be level shifted.

Fig. (16) shows an IXDD414 driving one IGBT of a Converter Brake Inverter (CBI) module. Here all protection features are incorporated. For High Temperature cutoff, a bridge circuit is used with the CBI module's thermistor. Comparator U3 compares voltage drop across the thermistor to the stable voltage from the Zener diode. P1 can be used to preset the cutoff point at which the comparator's output goes low. This is fed into the Microcomputer as OVERTEMP signal.

Short circuit protection is provided by continuously monitoring the voltage drop across a SHUNT. Note that one end of SHUNT is connected to the power supply ground GND1. The voltage picked up from this SHUNT is amplified by a low noise Op Amp and is then compared to the stable voltage from the same Zener. When short circuit occurs, the comparator output (FAULT) goes low. 1% metal film resistors are used throughout in both these circuits to ensure precision and stability. C3 and C4 help in offering low pass filtering to avoid nuisance tripping.

Principle of DESAT sensing for detecting overload on an IGBT has been explained before in section 2.5 above. In the case of AC Motor Drive, each IGBT has to be protected from overload using separate DESAT sensing. Fig. (16) and Fig. (17) show the connection for each IGBT. DESAT sensing is done on the isolated side of each opto-coupler, while the resultant FAULT signal is generated on the common input side with respect to GND1. Each FAULT signal is open collector type and hence can be tied together with other FAULT signals from other opto-coupler or from other comparators. The Microcomputer will stop output drive signals when either FAULT or OVERTEMP signal goes low. When this happens, notice that IXDD414 offers a -ve bias of -5V to guarantee turn-off conditions, even in presence of electrical noise. -5V is applied to gate of each IGBT during turn-off even under normal operating conditions. After fault is cleared, the Microcomputer can issue a RESET signal for resuming normal operation.

5.0 PRACTICAL CONSIDERATIONS

When designing and building driver circuits for MOSFET/IGBT, several practical aspects have to be taken care of to avoid unpleasant voltage spikes, oscillation or ringing and false turn-on. More often than not, these are a result of improper or inadequate power supply by-passing, layout and mismatch of driver to the driven MOSFET/IGBT.

As we understand now, turning MOSFET/IGBT on and off amounts to charging and discharging large capacitive loads. Suppose we are trying to charge a capacitive load of 10,000 pF from 0 to 15 VDC (assuming we are turning on a MOSFET) in 25 ns, using IXDD414, which is a 14 amp ultra high speed driver.

$$I = \triangle V \times C / \triangle t \qquad \text{Eq. 5.1}$$

$$I = (15-0) \times 10000 \times 10^{-12} / 25 \times 10^{-9} = 6 \text{ A}$$

What this equation tells us is that current output from driver is directly proportional to voltage swing and/or load capacitance and inversely proportional to rise time. Actually the charging current would not be steady, but would peak around 9.6 Amps, well within the capability of IXDD414. However, IXDD414 will have to draw this current from its power supply in just 25 ns. The best way to guarantee this is by putting a pair of by-pass capacitors (of at least 10 times the load capacitance) of complementary impedance curves in parallel, very close to the V_{CC} pin of IXDD414. These capacitors should have the lowest possible ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). One must keep the capacitor lead lengths to the bare minimum.

Another very crucial point is proper grounding. Drivers need a very low impedance path for current return to ground avoiding loops. The three paths for returning current to ground are: 1. Between IXDD414 and the logic driving it; 2. Between IXDD414 and its own power supply; 3. Between IXDD414 and the source/emitter of MOSFET/IGBT being driven. All these paths should be extremely short in length to reduce inductance and be as wide as possible to reduce resistance. Also these ground paths should be kept distinctly separate to avoid returning ground current from the load to affect the logic line driving the IXDD414. A good method is to dedicate one copper plane in a multilayered PCB to provide a ground surface. All ground points in the circuit should return to the same physical point to avoid generating differential ground potentials.

With desired rise and fall times in the range of 25 to 50 ns, extreme care is required to keep lengths of current carrying conductors to the bare minimum. Since every inch of length adds approximately 20 nH of inductance, a di/dt of 240 Amps/microsecond (used in the example calculation for Eq. 5.1) generates a transient LdI/dt voltage of 4.8 volts per inch of wire length, which subtracts from the driver's output. The real effect will be a significant increase in rise time for every tiny increase in conductor length from output pin of driver to the Gate lead of MOSFET/IGBT. For example, one extra inch of conductor length could increase rise time from 20 ns to 70 ns, in a ultra high speed gate drive circuit. Another detrimental effect of longer conductor length is transmission line effect and resultant RFI/EMI.

It is prudent to also keep in mind the fact that every MOSFET/IGBT has some inductance depending on the package style and design. The lower this value, the better is

the switching performance, as this inductance is, in effect, in series with the source/emitter and the resulting negative feedback increases switching times. IXYS MOSFET/IGBTs are housed in packages, which have extremely low intrinsic inductance.

While applying driver IC for any application, it is also necessary to compute power dissipated in the driver for a worst case scenario. The total power dissipated in the driver IC is a sum of the following:

1. Capacitive load power dissipation;
2. Transition power dissipation;
3. Quiescent power dissipation.

For all IXDD series of drivers, transition power dissipation is absent due to a unique method (Patent pending) to drive the output N-Channel and P-Channel MOSFETs, practically eliminating cross conduction.

As described under section 1.4, a MOSFET/IGBT driver incurs losses. Let us derive formulae to compute this power loss in a driver:

$$P_{D(on)} = \frac{D \times R_{OH} \times V_{cc} \times Q_g \times f_{sw}}{R_{OH} + R_{Gext} + R_{Gint}} \quad \text{Eq. 5.2}$$

$$P_{D(off)} = \frac{(1-D) \times R_{OL} \times V_{cc} \times Q_g \times f_{sw}}{R_{OL} + R_{Gext} + R_{Gint}} \quad \text{Eq. 5.3}$$

where: R_{OH} = Output resistance of driver @ output High
R_{OL} = Output resistance of driver @ output Low
f_{sw} = Switching frequency
R_{Gext} = resistance kept externally in series with Gate of MOSFET/IGBT
R_{Gint} = Internal mesh resistance of MOSFET/IGBT
D = Duty Cycle (Value between 0.0 to 1.0)
Q_g= Gate Charge of MOSFET/IGBT

Total loss $P_D = P_{D(on)} + P_{D(off)}$

Note also that in general, R_{Gint} is small and can be neglected and that ROH = ROL for all IXDD drivers. Consequently, if the external turn-on and turn-off gate resistors are identical, the total driver power dissipation formula simplifies to:

$$P_D = P_{D(on)} + P_{D(off)} = \frac{R_{OH} \times V_{cc} \times Q_g \times f_{sw}}{R_{OL} + R_{Gext}} \quad \text{Eq. 5.4}$$

Let us review some examples.

1. Assuming that, we are driving an IXFN200N07 for a Telecom power supply application or for a UPS/Inverter application at a switching frequency of 20 kHz

2. R_{Gext} = 4.7 Ohms and gate supply voltage is 15V.

On page No. 2 of the IXDD408 Data sheet, we read the value of R_{OH} = 1.5 Ohms (Maximum). For Q_g, refer to Data Sheet of the IXFN200N07 from www.ixys.com and go to Gate Charge vs. V_{GS} curve and look for value of Q_g at Vcc = 15 V. You can read it as 640 nC. Substituting these values into Eq. 5.4 yields:

$$P_D = \frac{1.5 \times 15 \times 640 \times 20{,}000 \times 10^{-9}}{1.5 + 4.7}$$

P_D = 46.45 mW

Assuming an ambient of 50 °C in the vicinity of IXDD408PI, the power dissipation capability of IXDD408PI must be derated by 7.6mW/°C, which works out to be 190 mW. The maximum allowable power dissipation at this temperature becomes 975-190=785 mW. However, as calculated above, we will be dissipating only 46.45 mW so we are well within the dissipation limit of 785 mW.

If one increases f_{sw} to 500 kHz for a DC to DC Converter application, keeping other parameters the same as above, now the dissipation would be 1.16 W, which exceeds the specification for IXDD408PI. So in this case, it is recommended to use either the IXDD408YI (TO-263 package) or IXDD408CI (TO-220) package. Both these packages can dissipate about 17 W with proper heat sinking arrangement. The TO-263 is a surface mount package and can be soldered onto a large pad on a copper surface of a PCB for achieving good heat transfer. For TO-220 package, a heat sink can be employed.

Let us take another example of a boost converter, using IXFK55N50 at V_{DS} = 250 VDC and at I_D = 27.5 Amps. Assuming f_{sw} = 500 kHz, Vcc = 12 V. From the curve of Gate Charge for IXFK55N50 in the Data Sheet one can determine that Q_g = 370 nC. Let us set R_{Gext} = 1.0 Ohm. We use IXDD414YI or IXDD414CI here, which can dissipate 12W. Here typical value of $R_{OH} = R_{OL}$ = 0.6 Ohm. Substituting the above values in our equation, we compute the power dissipation to be:

$$P_D = \frac{0.6 \times 12 \times 370 \times 500 \text{ kHz} \times 10^{-9}}{0.6 + 1.0 + 0.0}$$

P_D = 0.83 W.

With adequate air circulation, one may be able to use the PDIP Package.

For the third example, considering driving the large size MOSFET module VMO 580-02F at f_{sw} = 250 kHz. Let Vcc = 10 V, $R_{OH} = R_{OL}$ = 0.6 Ohm, R_{Gext}= 0.0 Ohm. We read that Q_g =2750 nC at Vcc = 10 V off the VMO 580-02F data sheet. Now:

$$P_D = \frac{0.6 \times 10 \times 2750 \times 250kHz \times 10^{-9}}{0.6 + 0.0 + 0.0}$$

P_D = 6.86 W

IXDD414YI (TO-263) or IXDD414CI (TO-220) can easily drive this load provided adequate heatsinking and proper air flow is maintained. Comments above for mounting TO-263 and/or TO-220 packages apply here as well. For derating use 0.1 W/°C. So for an ambient temperature of 50 °C, it works out to be 2.5 W. As the limit of IXDD414YI or IXDD414CI is 12 W, subtracting 2.5 W from this yields 9.5 W. So 6.86 W is still possible. Thermal Impedance (Junction to Case) is 0.55°C/W for TO-263 and TO-220, hence a rise in case temperature should be within limit. If we increase Vcc to 15V, conduction losses in MOSFET could reduce due to lower R_{DS}(on), but obtaining the same rise and fall times will incur more power loss in driver due to increased Vcc and Qg. If that happens, approach described in Fig. (14) can be employed.

6. CONCLUSION

With proliferating applications of modern power electronics worldwide, faster, more efficient and more compact MOSFETs and IGBTs are replacing older solid state and mechanical devices. The design of newer and more efficient techniques to turn these solid state devices on and off is a subject that requires thorough study and understanding of the internal structure and dynamic processes involved in the working of MOSFET/IGBTs.

Main emphasis in modern Power Electronics is to reduce total losses dissipated in devices and subsystems for higher operating efficiency and achieving more compact designs, reducing volume and weight of resultant systems. Thus, operation at higher and higher switching frequencies is now a necessity, and as a result, switching losses predominate in the power-loss-budget in semiconductor switches. Reducing switching losses then becomes the single most crucial goal. Keeping this goal in mind, the entire line of IXYS MOSFET/IGBT Drivers are designed to facilitate the design of drive circuits that yield fast rise and fall times, matching or often exceeding the speeds of the driven MOSFET/IGBTs. Extremely low propagation delay time facilitates implementation of fast overload/short circuit protection.

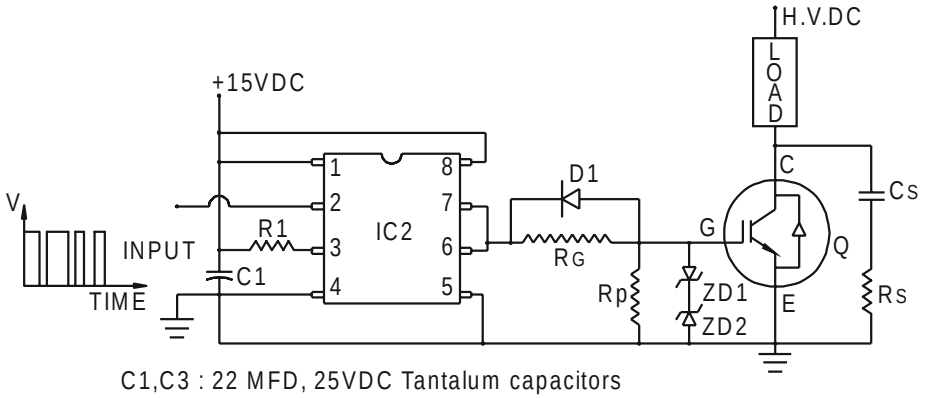
With the advent of IC Drivers for these fast MOSFET/IGBTs, the designer is relieved of the tedious task of designing elaborate driver circuits. Nevertheless, understanding these newer ICs, their strengths and limitations, is of paramount importance. Different configurations for particular topologies call for specific application knowledge. Illustrations are the best way to explain theory and applications of these IC drivers. Practical use of these IC drivers call for great care for achieving near theoretical results.

References:

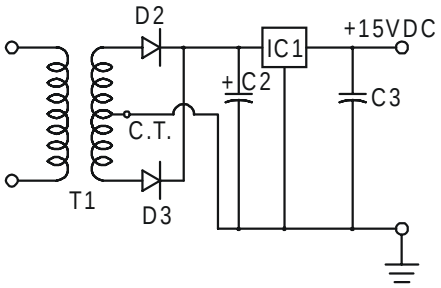
1. B. Jayant Baliga, “Power Semiconductor Devices”, PWS Publishing Company, Boston, MA (1996)
2. Ned Mohan, Tore M. Undeland, William P. Robbins: “POWER ELECTRONICS: Converters, Applications and Design”, John Wiley & Sons, New York (1994)
3. Power Supply Design Seminar - 2001 series, Unitrode Products from Texas Instruments.

Recommended for further reading:

1. George J. Krausse, “Gate Driver Design for Switch-Mode Applications and the DE-SERIES MOSFET Transistor”, Directed Energy, Inc. Application Note available from<www.directedenergy.com>.



C1,C3 : 22 MFD, 25VDC Tantalum capacitors
C2 : 2200 MFD, 35VDC Electrolytic capacitors
T1 : 220 VAC to 15-0-15 VAC, 15VA control transformer
110VAC TO 15-0-15
Q : IXLF19N250A



IC1 : 7815 Regulator
IC2 : IXDD408 or IXDD414
D1 : IN5817
D2,D3 : IN4002
ZD1,ZD2 : 18V, 400MW ZENERS
RG1 : 3.3 ohms to 27 ohms
depending on Turn-ON speed
Rp : 2K2, ¼ W, 5%
Cs,Rs : Snubber network to reduce IGBT switching losses. Value depends upon fsw. Suggest: Cs=0.1 MFD, Rs=10 to 33 ohms
R1 : 10K, ¼ w

Fig. (8) Circuit schematic showing how to use IXDD408 or IXDD414 to drive an IGBT

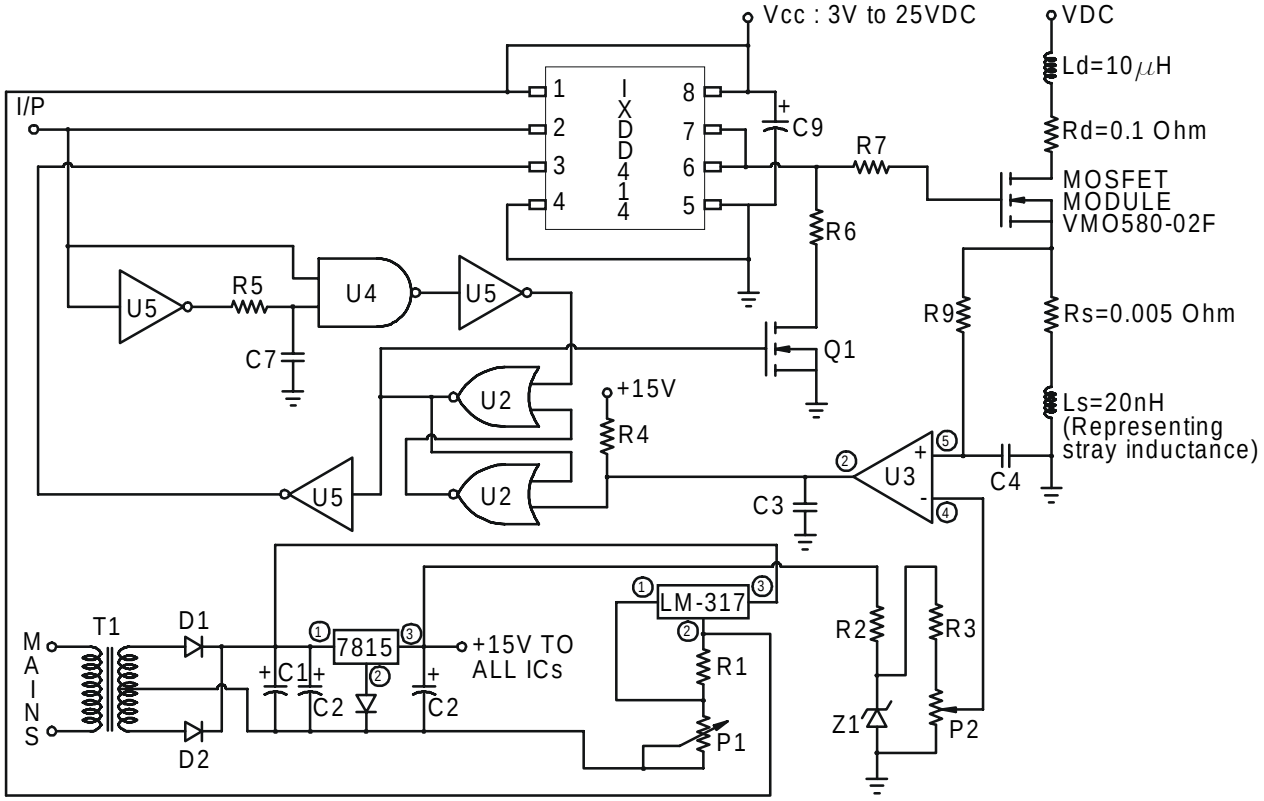


Fig. (9). Evaluation circuit to test IXDD408/IXDD414 for soft turn off.

Bill of Materials for Fig.(9)

Resistors:
R1: 240
R2: 560
R3: 10K
R4: 5K
R5: 1Meg
R6: 1K5
R7: Rg-T.B.D.
R8: 1Meg

Capacitors:

C1: 1000mF;35VWDC
C2: 22mF, 63 VWDC
C3: 1pF, silver dipped mica
C4: 100pF silver dipped mica
C5: 0.1mF, 35WDC Tantalum
C6: 0.1mF, 35VWDC Tantalum
C7: 1pF silver dipped mica
C8: 0.1mF, 35VWDC Tantalum
C9: 0.1mF, 35VWDC Tantalum
C10: 0.1mF, 35VWDC Tantalum

Trimmers:
P1: 5K, 3006P Bourns or Spectrol
P2: 1K, 3006P Bpurns or Spectrol

Diodes:
D1: 1N4002 or BA 159
D2: 1N4002 or BA 159

Zener Diodes:
1. Z1: 1N821

Voltage Regulators:
1. 7815
2. LM317T

Transistors:
1. Q1: 2N7000

ICs:
U1: IXDD408PI or IXDD414PI
U2: CD4001
U3: LM339
U4: CD4011
U5: CD4049
U6: IXDD408YI or IXDD414YI
Note: Either use either U1 or U6 but not both.

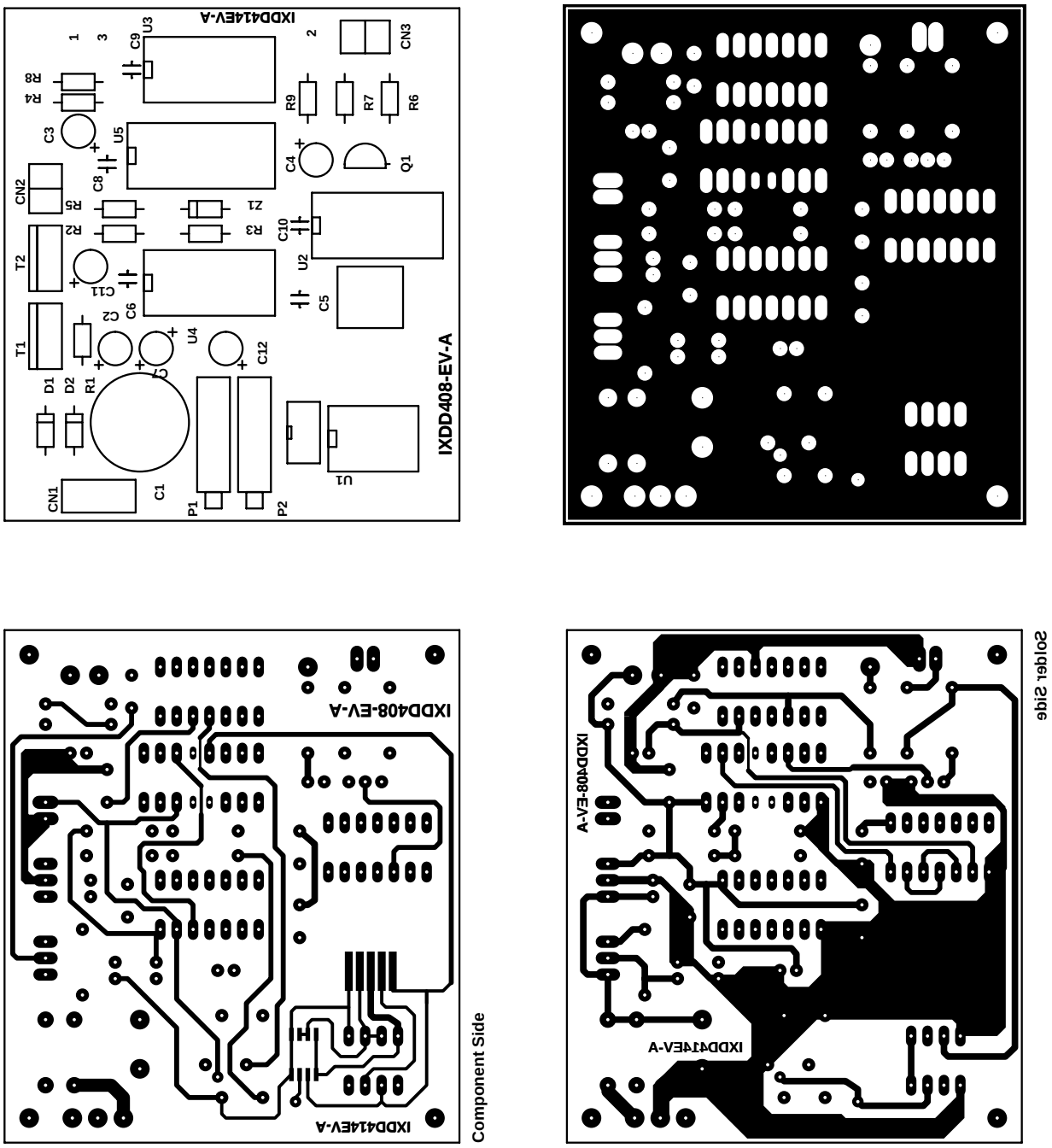


Fig. (10). +ve and -ve and component layout with silk sceen diagram.

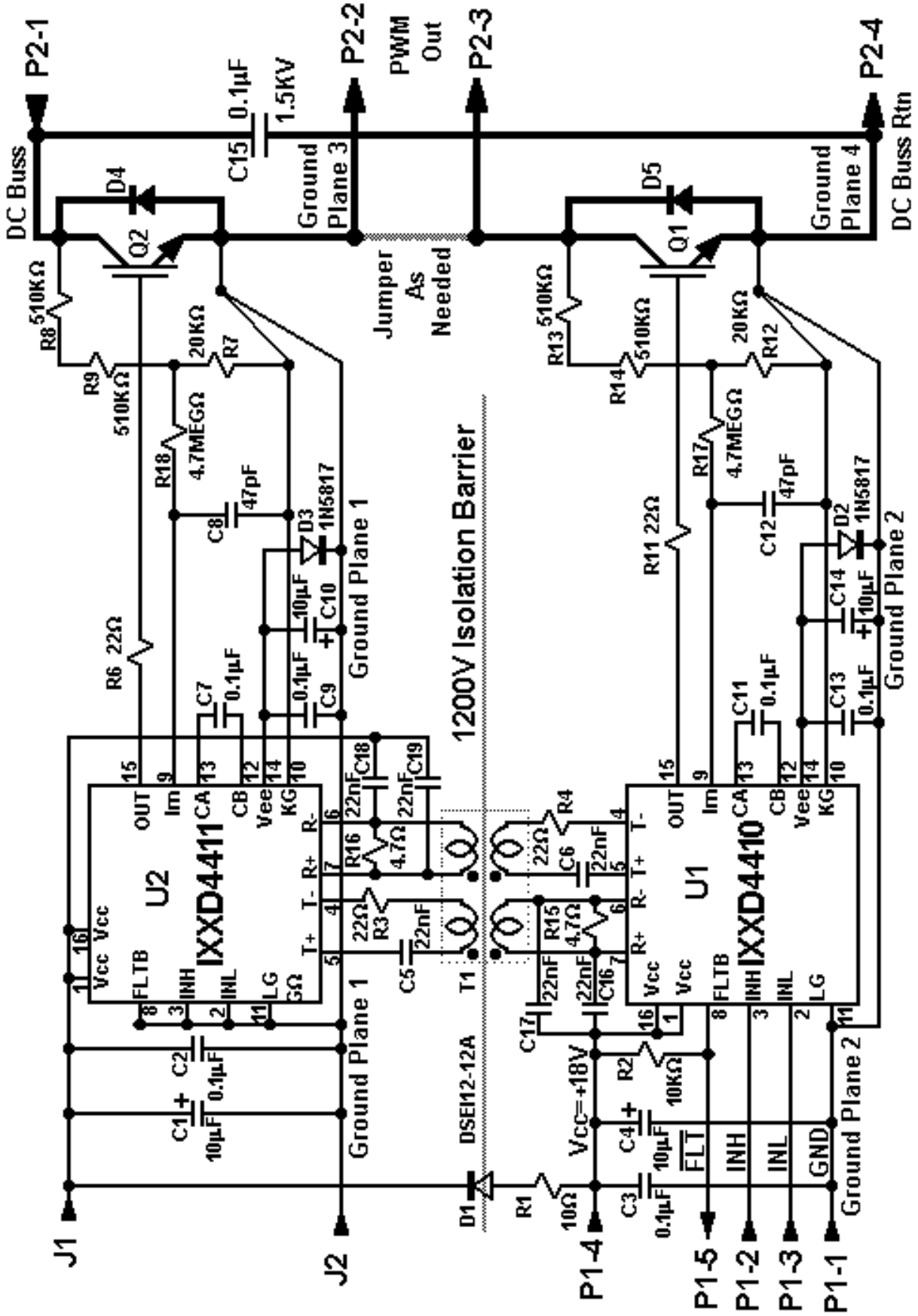


Fig. 11. IXBD4410/4411 Evaluation Board Schematic.

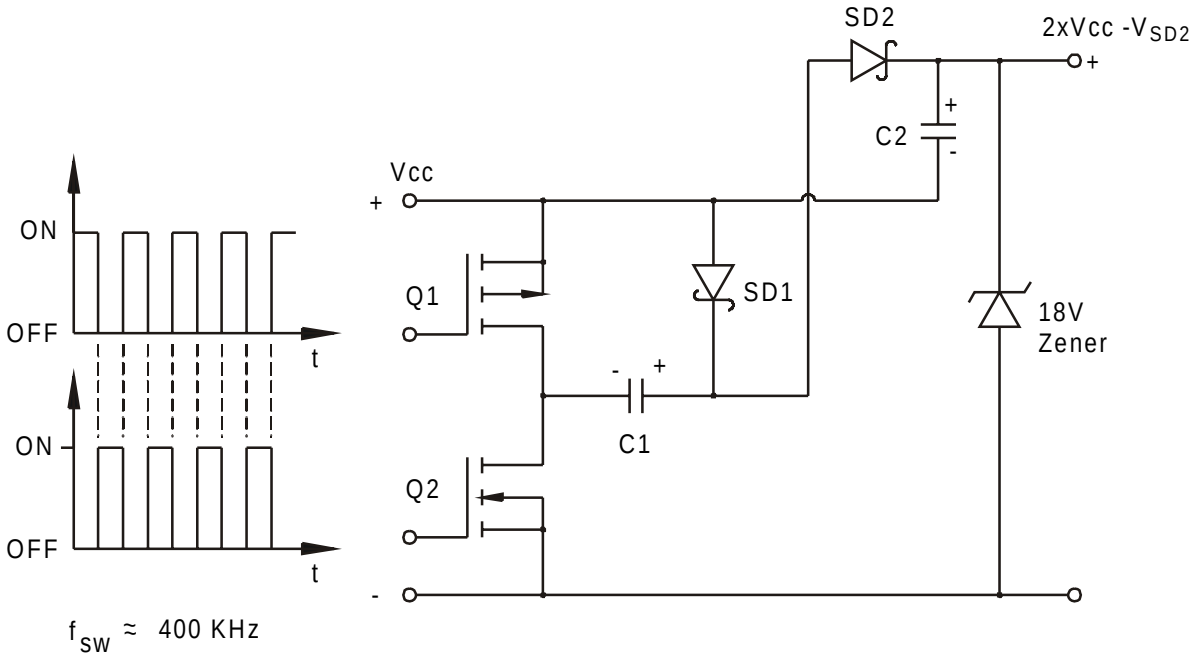
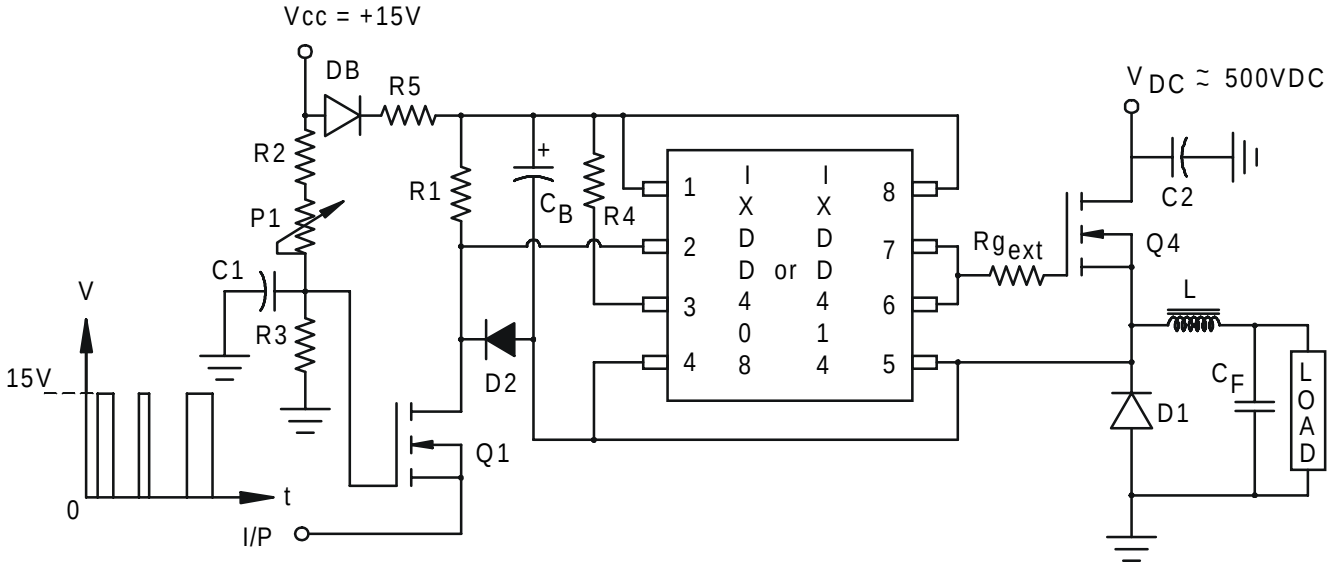


Fig. (12A) Basic Charge Pump Doubler



Q1 : IXTU01N100
DB : DSEP9-06CR
D1 : DSEC60-12A
D2 : 1N5817
C1 : 20MFD,25V
C2 : 20MFD,1000 Volts,CSI 10DC0020
CB : 10MFD,25VDC
P1 : 5K Trim pot

Rg$_{ext}$: 1.0 Ohm to 4.7 Ohm
CF : GE A28F5601
0.1MFD,1000 Volts
R1 : 1K
R2 : 10K
R3 : 2K
R4 : 10K
R5 : 1 Ohm
L : 5µH,DALE IH-5

Fig. (12B) Basic bootstrap gate drive technique

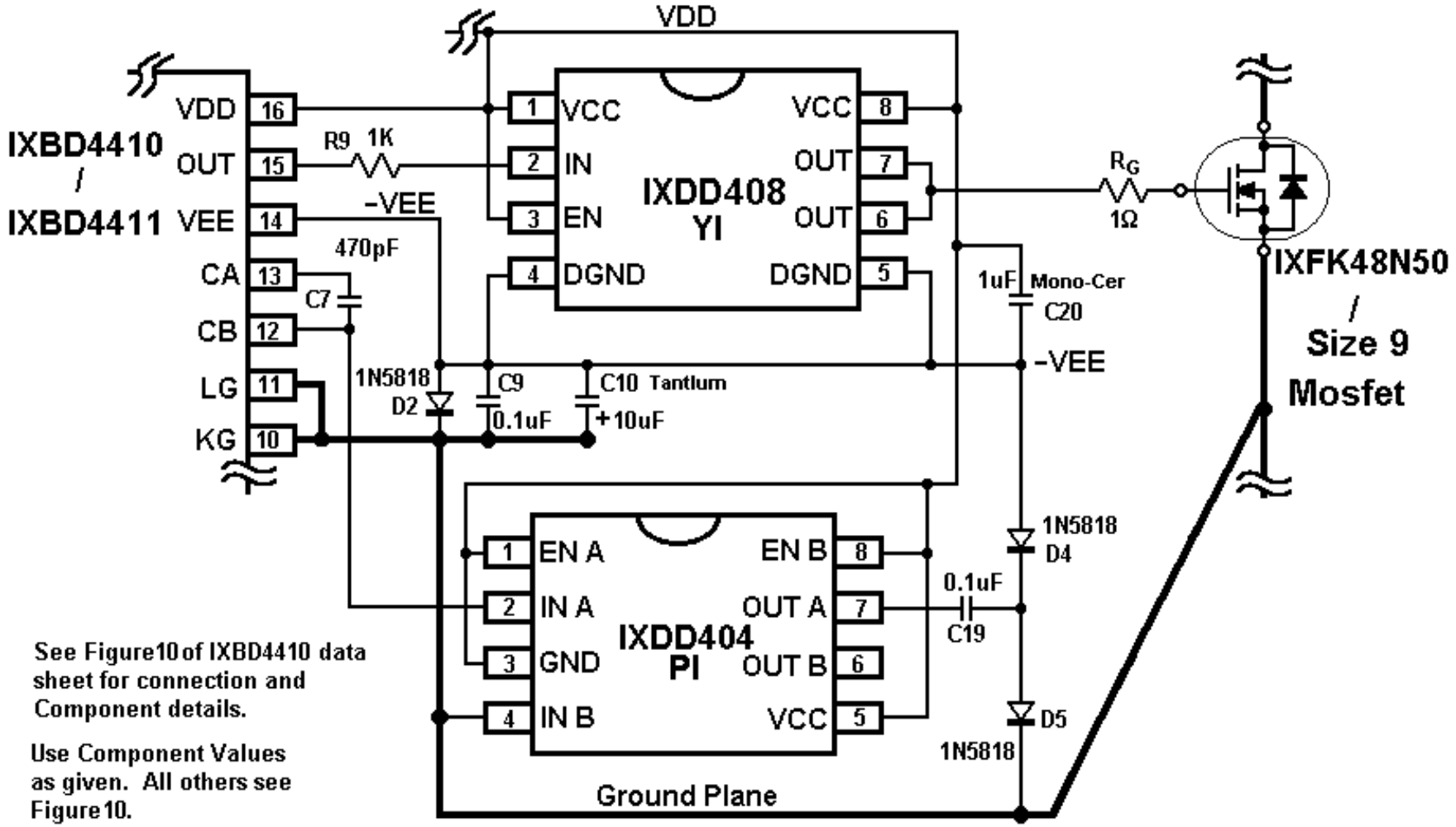


Fig. (12C). Boosting output gate drive to +/-8 A and charge pump output to 350mA for 400kHz switching of size 9 devices with the IXBD4410/4411 gate driver chip set.

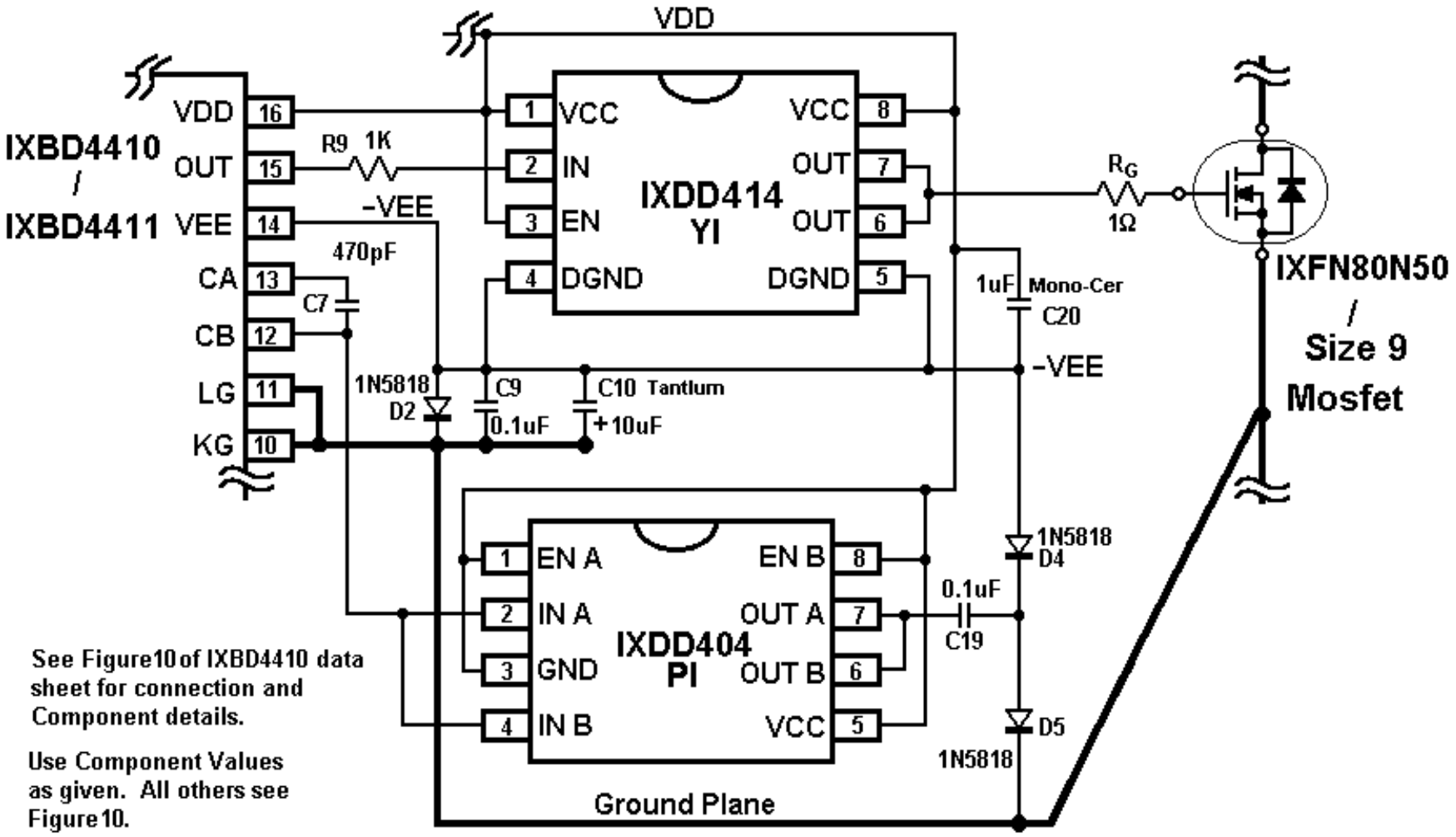


Fig. (12D). Boosting ouptput gate drive to +/-14 A and charge pump output to 500mA for 400kHz switching of size 9 devices with the IXBD4410/4411 gate driver chip set.

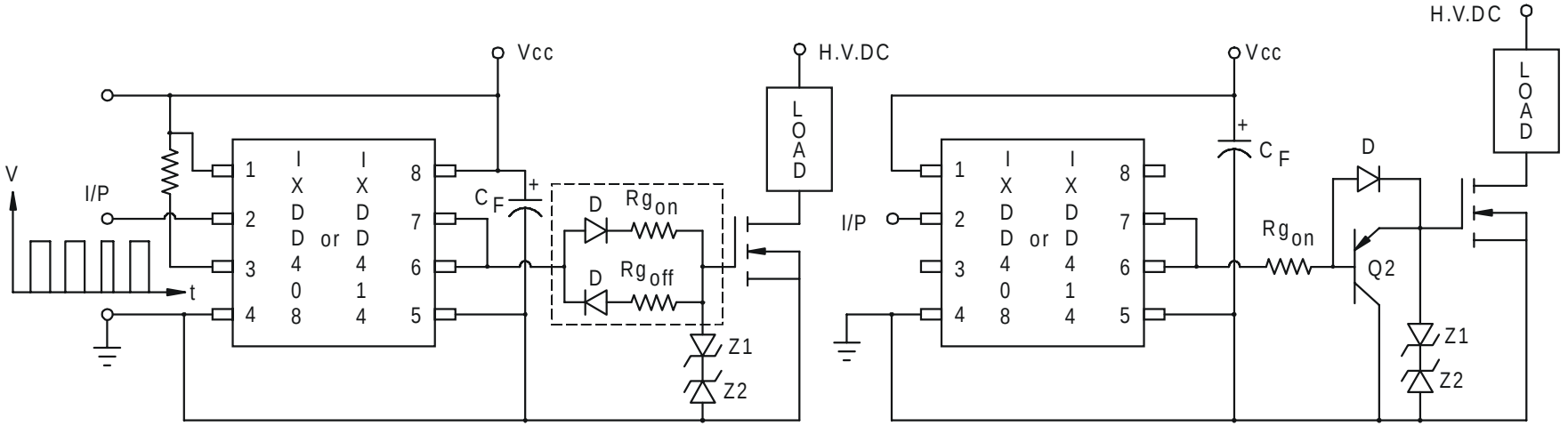


Fig (13) Turn-off enhancement methods.

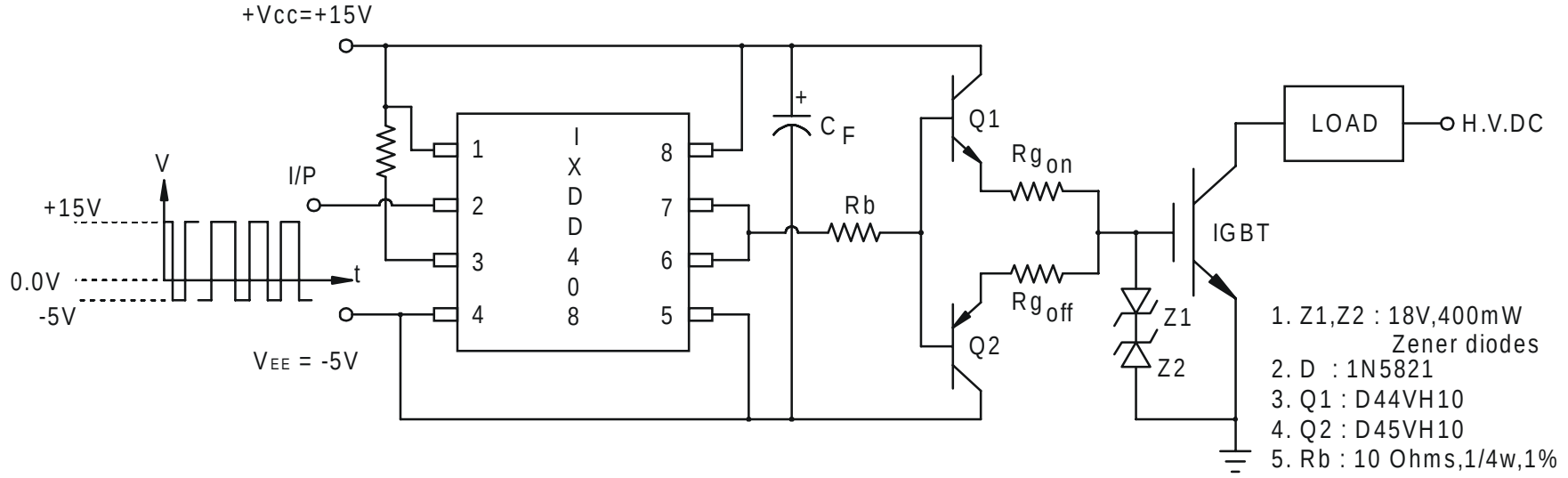


Fig. (14). Technique to boost current output and provide -ve bias to achieve faster turn off for high power MOSFET and IGBT Modules

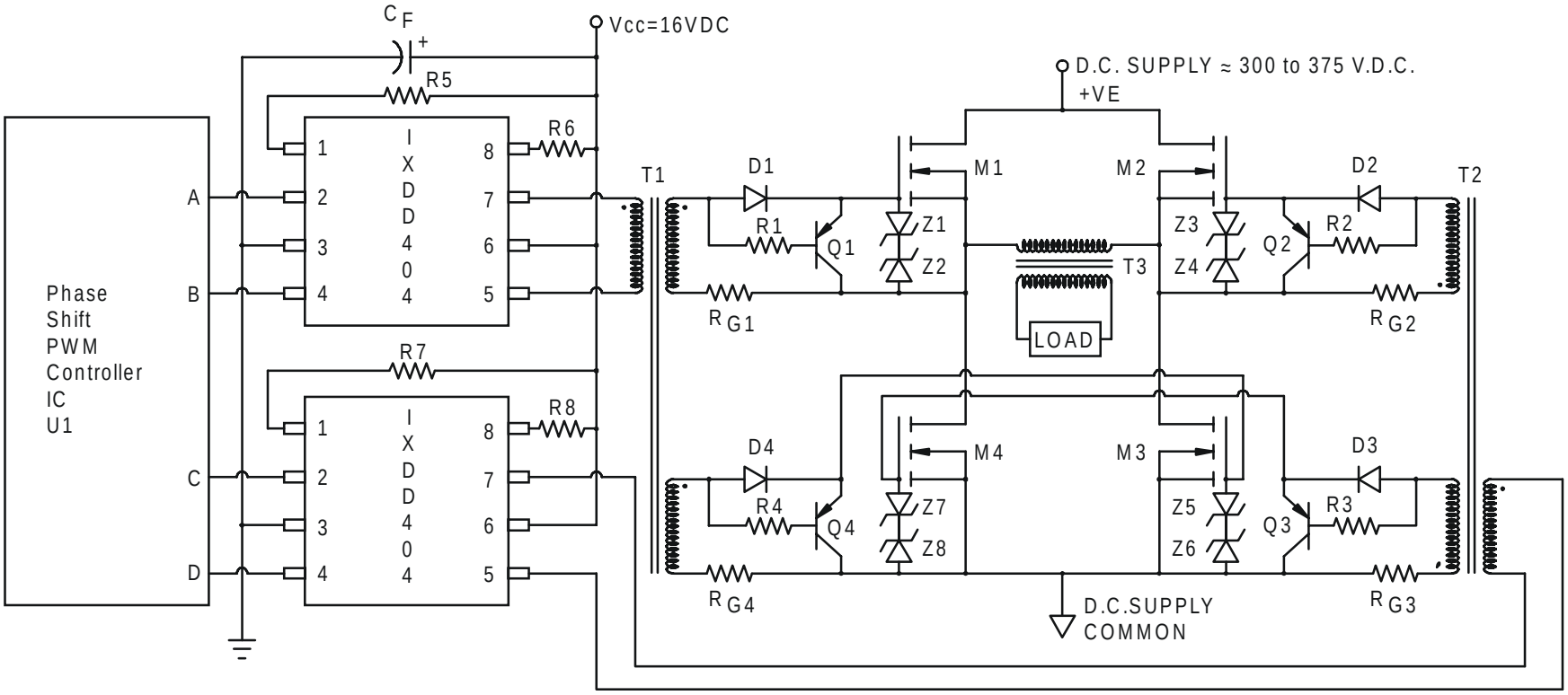


Fig. (15) Transformer coupled Gate Drive arrangement for "H" Bridge in a Phase Shift PWM Controller at fixed Switching frequency.

SUGGESTED PARTS:

1. U1 : T.I. UC3879
2. T1,T2 : Coilcraft Part No. SD250-3
3. Q1,Q2,Q3,Q4 : 2N2905A
4. D1,D2,D3,D4 : DSEP8-02A IXYS HiPerFRED
5. T3 : OUTPUT Transformer
6. CF : 22MFD,35 VWDC Tantalum Capacitor
7. R1,R2,R3,R4 : 560 Ohms, ¼ w,1% Metal film
8. M1,M2,M3,M4 : IXFN55N50 IXYS HiPerFET or IXFN80N50 IXYS HiPerFET
9. Z1,Z2,...Z8 : 18V, 400mW Zener diodes.
10. RG1,RG2,RG3,RG4 : 3.3 Ohms, ¼ w, 1% Metal Film resistors.
11. R5,R6,R7,R8 : 10K, ¼ w, 5%

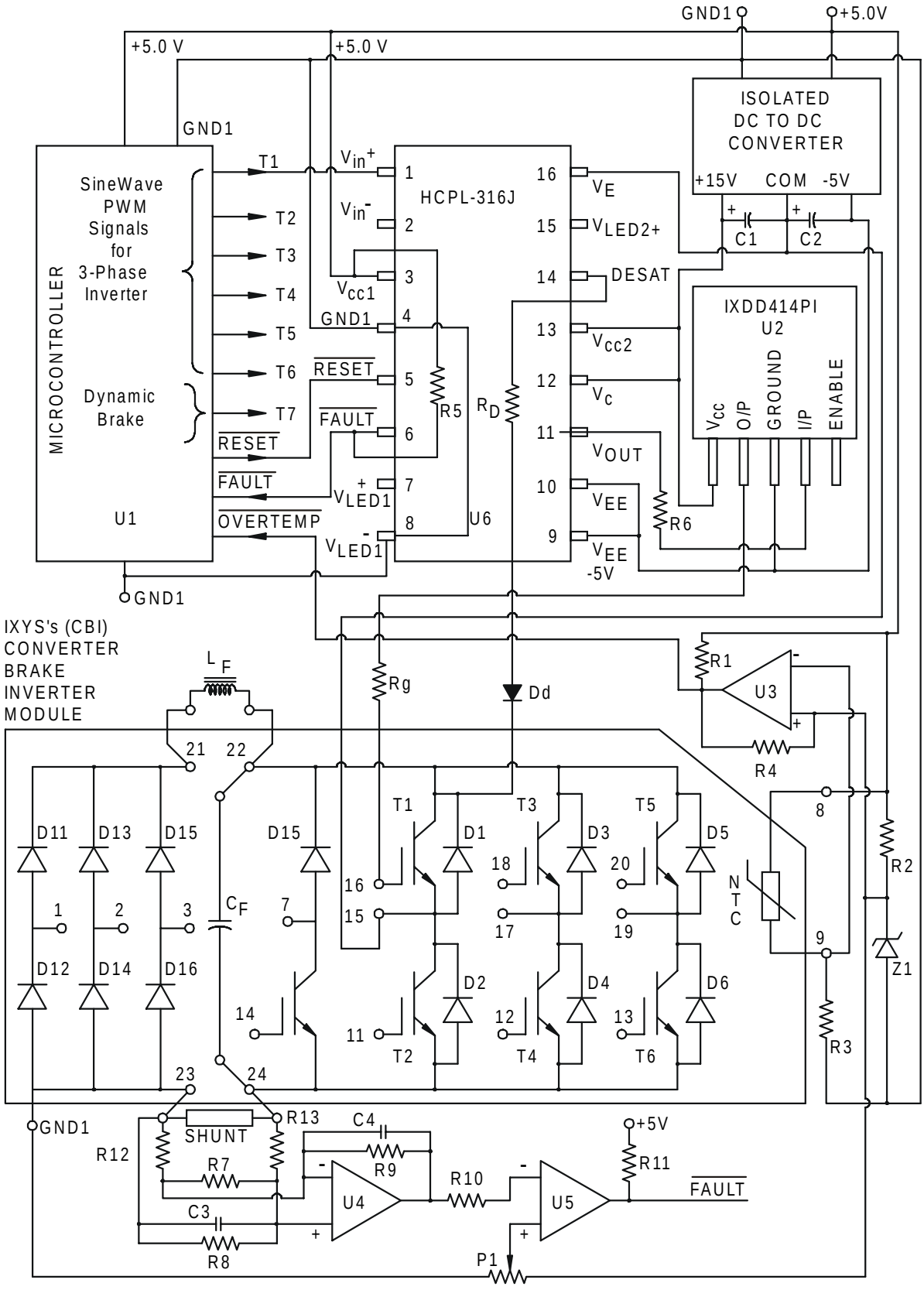
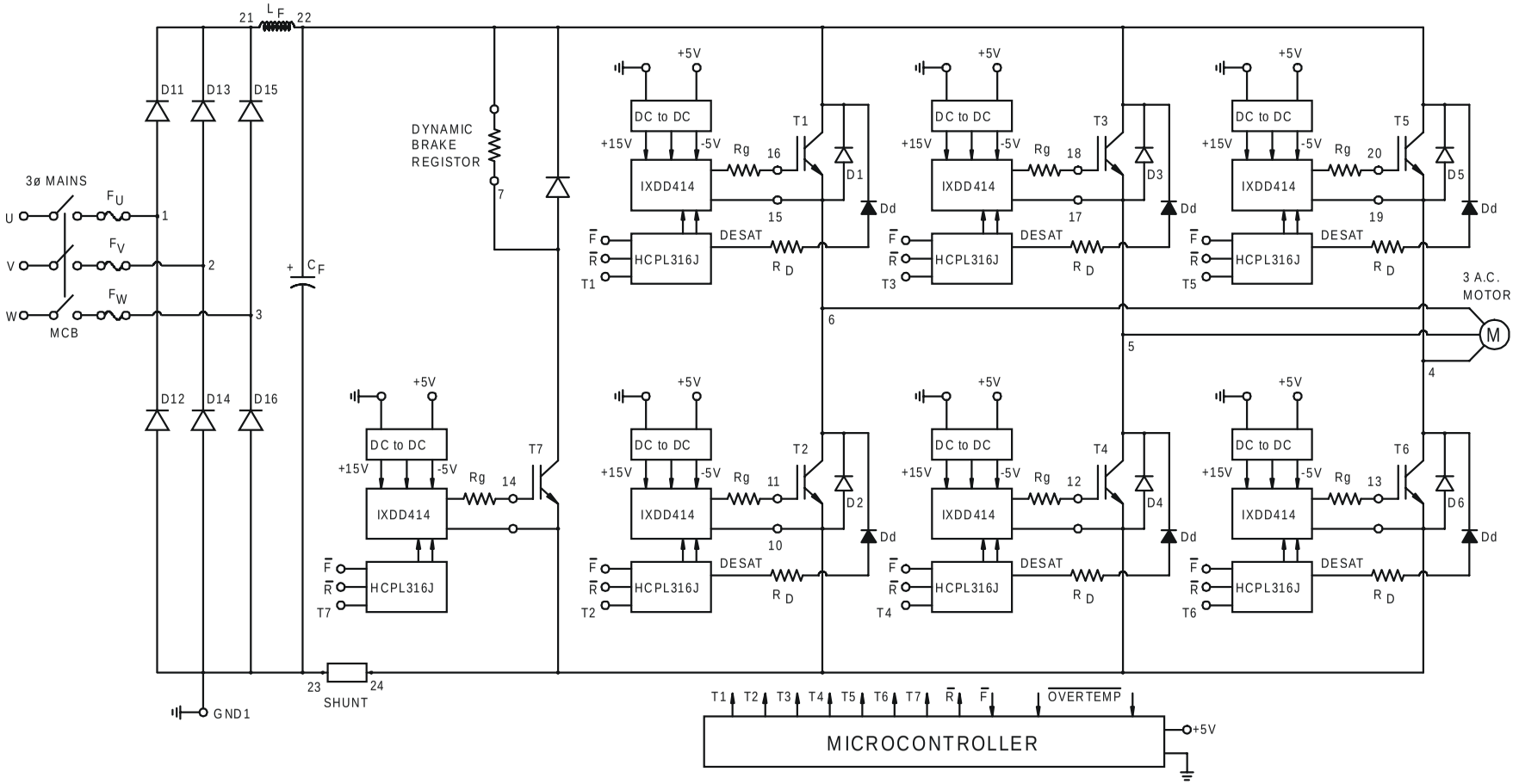


Fig. (16) 3-Phase AC Motor drive schematic showing how IXYS CBI (Converter-Brake-Inverter) Module can be driven by IXDD414 using opto-couplers.
All protection features are incorporated.

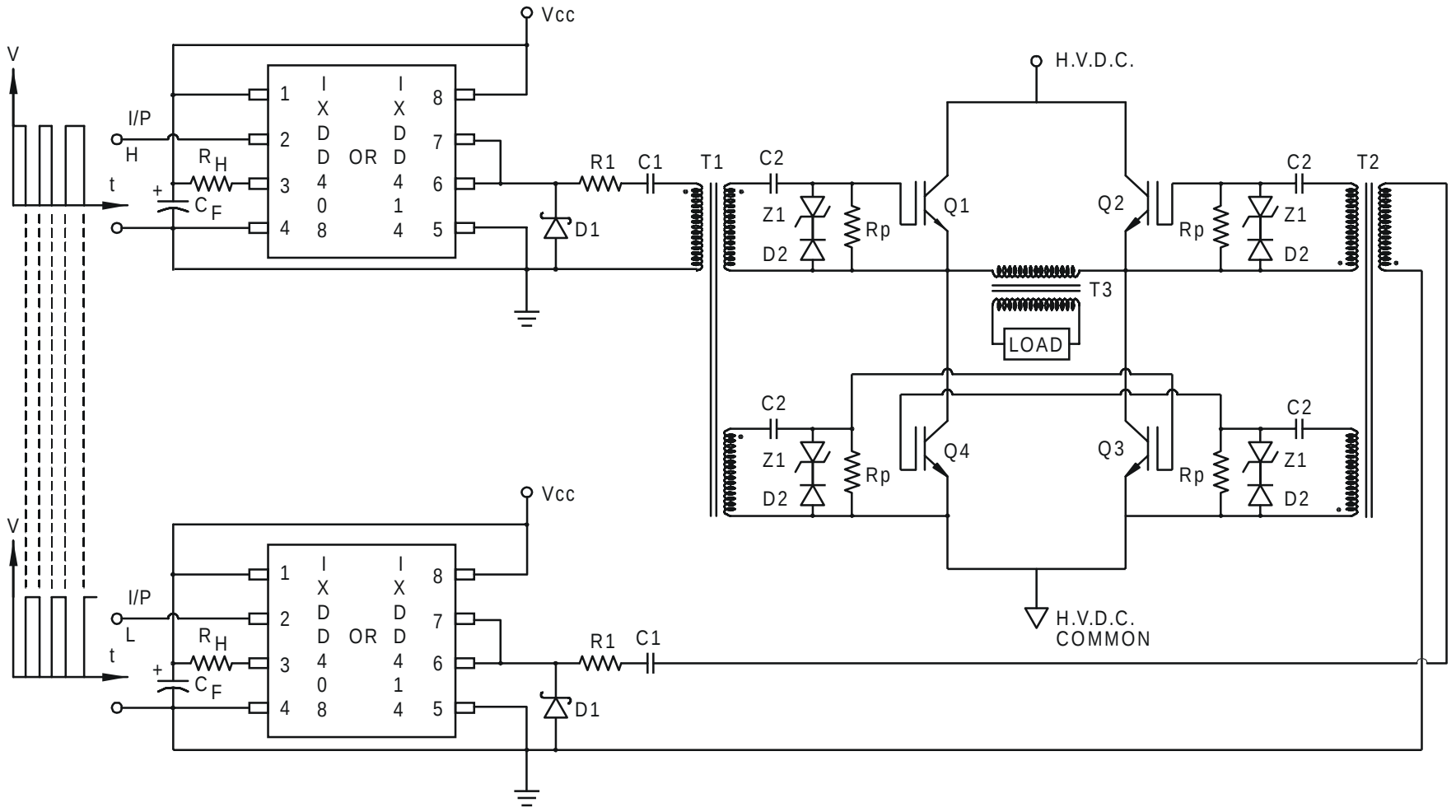


NOTES: 1. ALL $\overline{F}$ = $\overline{FAULT}$ SIGNALS ARE TIED TOGETHER (BEING OPEN COLLECTOR) AND FED INTO MICROCOMPUTER.
2. ALL $\overline{R}$ = $\overline{RESET}$ SIGNALS ARE TIED TOGETHER AND FED TO HCPL-316J.
3. $\overline{OVERTEMP}$ AND OVERLOAD/SHORT CIRCUIT $\overline{FAULT}$ SIGNALS ARE GENERATED AS PER FIG(16)
$\overline{OVERTEMP}$ IS ALSO FED IN MICROCOMPUTER.

FIG(17) IXYS CONVERTER, BRAKE INVERTER (CBI) MODULE BEING DRIVEN BY IXDD414 WITH OPTO-COUPLER AND DESAT, OVERTEMP AND SHORT CIRCUIT/OVERLOAD PROTECTIONS.

Bill of Materials for Fig. (16) and Fig. (17)

R1, R3, R5, R10, R11: 10K, 1/4W, 1% MFR
R2: 560 Ohms, 1/4W, 1% MFR
R4: 2.2 MegOhms, 1/4W, 5%
R6: 100 Ohms, 1/4 W, 1% MFR
R7: 20K, 1/4W, 1% MFR
R8, R9: 61.9K, 1/4W, 1% MFR
R12, R13: 1.24K, 1/4W, 1% MFR
Rg: T.B.D. based on Ton and Toff & size of IGBT
R_D:100 Ohms,1/4 w, 5%
P1: 10K, multi turn trimpot, Bourns 3006P or Spectrol
C3, C4: 33 pF, silver dipped mica
Dd: General Semiconductor make,
Type: RGP02-20E, 0.5 A, 2000 V, trr: 300 ns
Z1: Zener LM336, 2.5 Volt
U3, U5 : LM339 Comparator
U4 : LM-101 Op Amp
SHUNT : 75 mV @ full load current
LF: Gapped D C Choke for filtering rectified power
CF: Electrolytic Filter Capacitor with very low ESR & ESL and screw type terminals to handle high ripple current. Voltage rating is based on DC Bus plus AC ripple Voltage
CBI Module: IXYS Corporation Type Nos:
MUBW 50-12A8 or any MUBW module from
CBI 1, CBI 2 or CBI 3 series.
Microcontroller: T.I. TMS320F240 with embedded software for AC Drive, using brake feature.
IXDD414 Driver chip: 7 are required to implement the A.C.Drive, using Brake feature.
HCPL316J(Opto-coupler) : 7 are required to implement the A.C.Drive With Brake feature.
Isolated DC to DC Converter: 7 are required with specified isolation.



FIG(18) A Transformer coupled Gate Drive circuit employing D.C. restore technique and showing how to generate -ve bias during turn-off.